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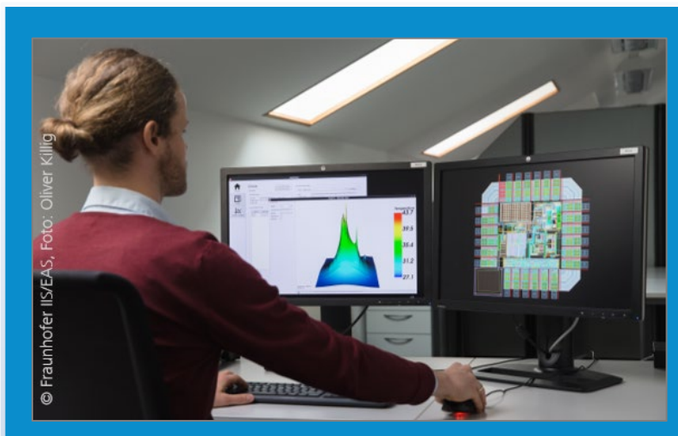
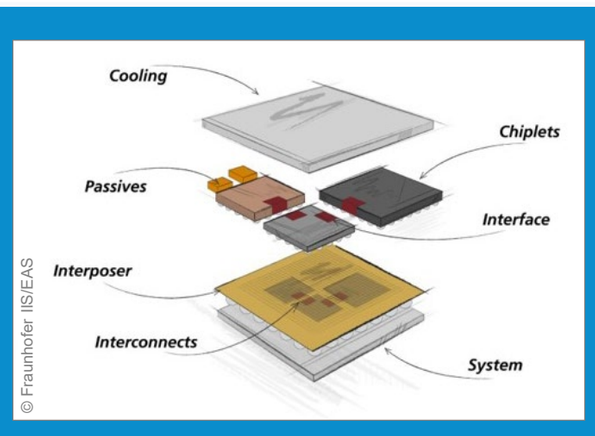
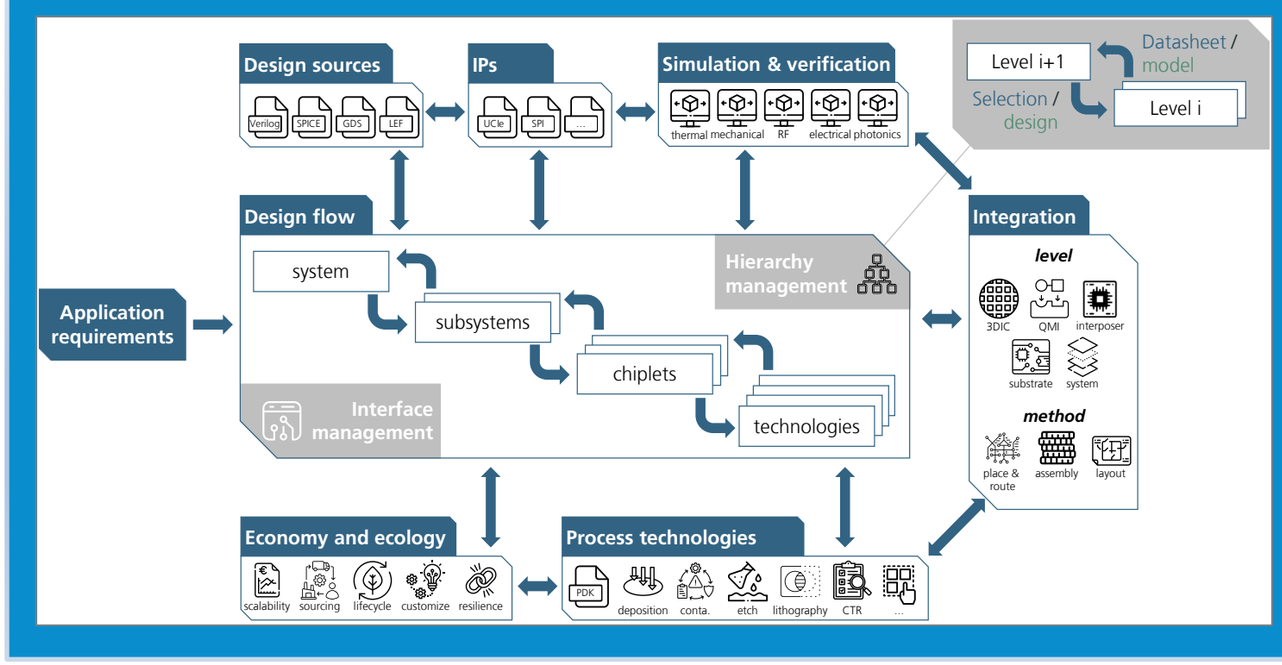
System Technology Co-Optimisation (STCO)







Introduction

STCO is a holistic strategy for enhancing heterogeneous electronic systems. This design approach improves the predictability and implementation of system properties. It integrates various methods to facilitate ground-breaking design solutions that can significantly boost the performance, increase efficiency, and lower costs of heterogeneous and chiplet-based modules.

The holistic STCO approach targets:

- Access to chiplets & advanced system integration technologies
- Cost/benefit analysis for heterogenous systems
- Utilization and optimization for demonstrator systems design: HPC, Sensing, Photonics, RF.

It utilises and enables:

- Systematic design approach for chiplets, 2.5/3D integration and Quasi-Monolithic Integration (QMI)
- Integration and utilization across a large design space
- Link to the EU design platform
- Contributions to IP and chiplet standards

Design Procedures, Links, and Interfaces

Currently, workflows and design flows are being defined including ADKs/PDKs with close link to test and manufacturing. This includes the utilization of interfaces that span across electrics IPs, the connection of software tools to seamless design flows, and the link between design & manufacturing. Furthermore, characterization and test is included in the design approach with DfX capabilities including: Design for Manufacturing (DfM), Design for Reliability (DfR), Design for Security (DfS), Design for Test (DfT).

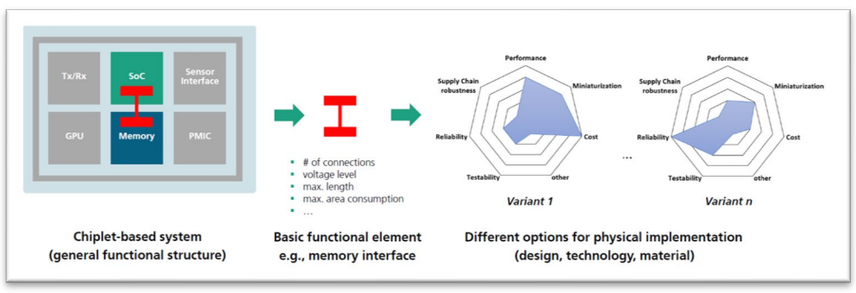
STCO Application & Access

STCO activities are closely linked to APECS Access. APECS STCO will be the methodological support to ease accessibility for EU companies to use new technologies and functionalities. It will cover:

- *chiplet design* with A/MS, digital, RF, MEMS, photonics,
- *advanced system integration* with panel-level, wafer-level & QMI,
- *semiconductor technology* from CMOS to SiGe, SiC, III-V, or LNOI.

Possible points of contact

- STCO workflow – identify benefits
- System-level analyses & prototypes
- IP and chiplet development
- Integration based on QMI / 2.5D / 3D
- Tool add-ons and flow development



Key questions to be discussed

1. Which are key KPIs in your development phase?
2. Which are the key challenges along your design process?
3. Which standards to you require STCO to comply with? (QM, interfacing, test, …)
4. Which requirements tools, modelling and design languages, and formats must be supported to fit your flows demands?
5. Which tools and/or tool compatibilities do you require?

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