APECS

Coordinated by

Fraunhofer

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Forschungsfabrik Mikroelektronik Deutschland

Pilot Line for Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems (APECS): STCO for 2.5 & 3D Integration

For a comprehensive STCO approach, an in-depth knowledge of the range of suitable technologies and their specific designs and properties is being built up. Also, short-comings of existing (state of the art) approaches can thus be highlighted to initiate innovations and RDI on such aspects

Panel Level System Integration utilizing Fan-Out Panel Technology
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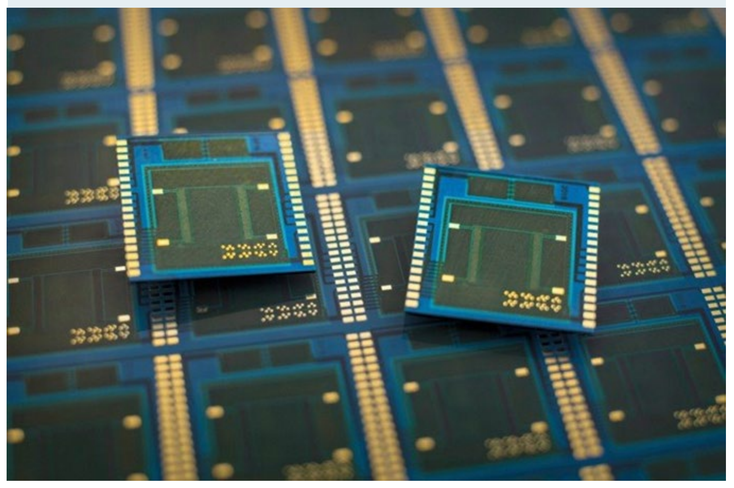

APECS 2.5&3D Integration Platform

The integration platform addresses three main aspects of the chiplet integration challenge:

- Interposers for the chiplet integration
- Interaction of chiplet modules
- Assembly of such modules to a functional (sub-)system

For this existing technology, toolboxes are complemented by novel concepts, innovations towards sub-micron resolutions and scalable system integration processes.

Functional Interposers for Chiplet Integration

For Advanced Node Semiconductors, interposers (offering highest integration densities) are required. This activity will innovate through silicon vias and the associated sub-micron resolution for multi level redistribution layers.
As not only ANS need to be integrated to realize a chiplet based system need to be addressed by this interposer technology, thus application dependent interposers have to be developed, namely non-silicon (e.g. glass, ceramic, SiC), organic (e.g. Flex, Advanced PCB and EMC based interposers) as well as interposers specifically designed to add functionalities to the system (passives (RCL), thermal management, structural protection)
Innovation targets included for the STCO paradigm therefore involve:

- Ultra high-density interposers based on 200-300mm Si platform, offering TSVs and re-routing for highest interconnect densities
- Non-Si interposers for special purposes like optica/LWG integration, MEMS/Sensor integration including Through X Vias (TXV), based on 200mm substrates
- Large format organic interposers up to 610mm

Glass interposer with TGVs and multi-layer RDL with assembled test chiplets
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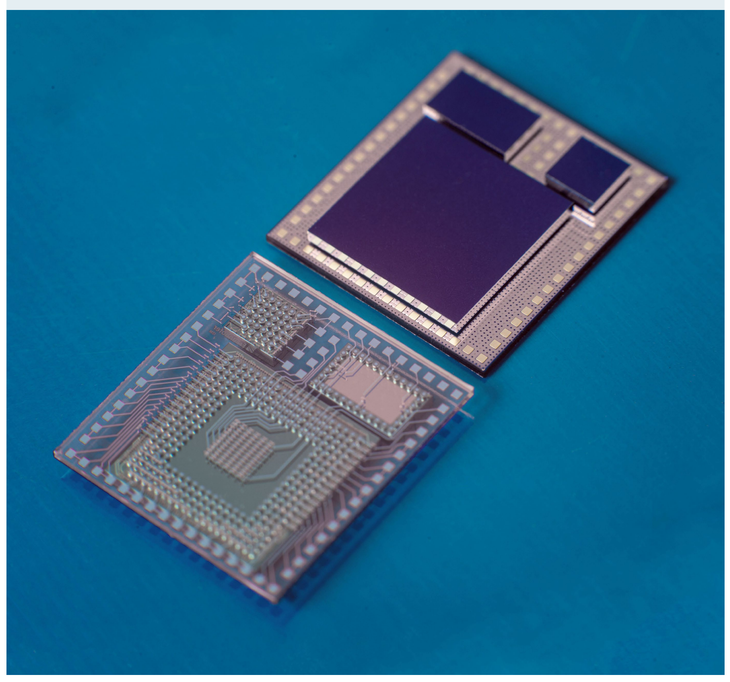

Functional Integration of Chiplets

Chiplets with their specific functionalities will still be based on established Si and WBG processes. Their interconnect layer thus need to be prepared – both in design as well in technology – to be compatible with the subsequent integration processes.
Especially looking into promising 3D integration techniques, preparation with micro bumps or highly controlled surface quality for hybrid bonding is key.
The integration processes with the respective interposers is performed on wafer or chiplet scale, depending on the system requirements. Requiring precising alignment, specific processes (like hybrid bonding) or even handling/assembly of extremely small chiplets with just several µm size bring up challenges both in process technology as well as the Design-for-Manufacturing and Design-for-Reliability paradigm.

3D Stack Integration by Die to Die to Wafer using micro bumps and TSVs
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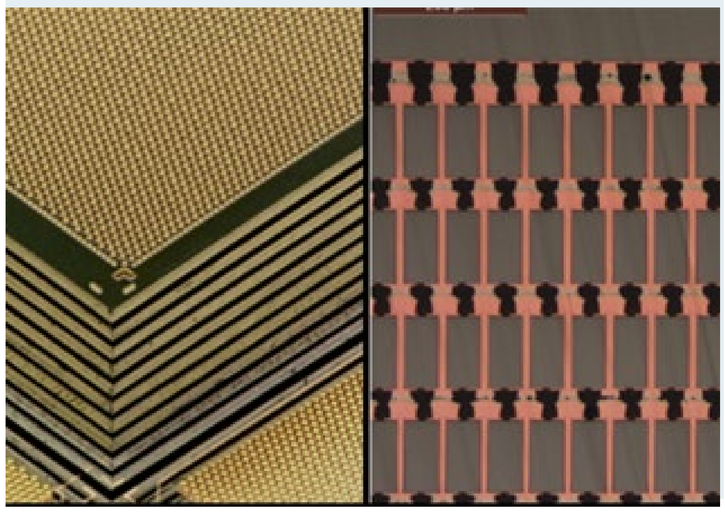

Assembly of Chiplet based Modules to HD Substrates

Such chiplet modules offer functionalities beyond an SoC, still require the connection on system level. Here, high density advances substrates with 10x smaller feature sizes compared to today´s state of the art will be the receiving part for such modules. Assembly technologies offered by EMS as of today will not anymore be adequate to cope with large area, high densitiy modules of this next generation of devices. Novel processes and radical innovations are expected to overcome this challenge, and APECS is addressing this:

- High speed and high precision assembly of chiplet modules to HD substrates with micron scale accuracy for large (~7cm) sized Si modules.
- Panel Level Systeme Integration using Fan-Out process, offering a “substrateless” built up of the system carrier with 2µm routing capabilities for unprecedented integration density on system level
- Layer-by-Layer integration, similar to wafer stacking, for full system functionalities which enable next generation neuromorphic computers with minimum latency and high efficiency

STCO Challenge

The integration of chiplets into a system offers new opportunities for highly functional, cost effective, secure and reliable devices.
However, to achieve this, newly surfacing challenges need to be addressed from the point of view of process engineering. Such innovations need to be integrated in a holistic STCO flow to get maximum benefit out of the innovative processes and architecture.
Building on established knowhow and a strong infrastructure, APECS will expand the knowledge and process capabilities towards hitherto unachievable targets, enabling the European industry to be at the forefront of microelectronic innovations.

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Additional information

The APECS consortium brings together the technological competences, infrastructure, and know-how of ten partners from eight European countries:
Germany (Fraunhofer-Gesellschaft as coordinator, FBH, IHP), France (CEA-Leti), Belgium (imec), Finland (VTT), Austria (TU Graz), Greece (FORTH), Spain (IMB-CNM, CSIC) and Portugal (INL).

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