The Demonstrators of the APECS Pilot Line

High Performance Computing – Multi Material Sensor – Optical Transmitter – Radio Frequency Solutions

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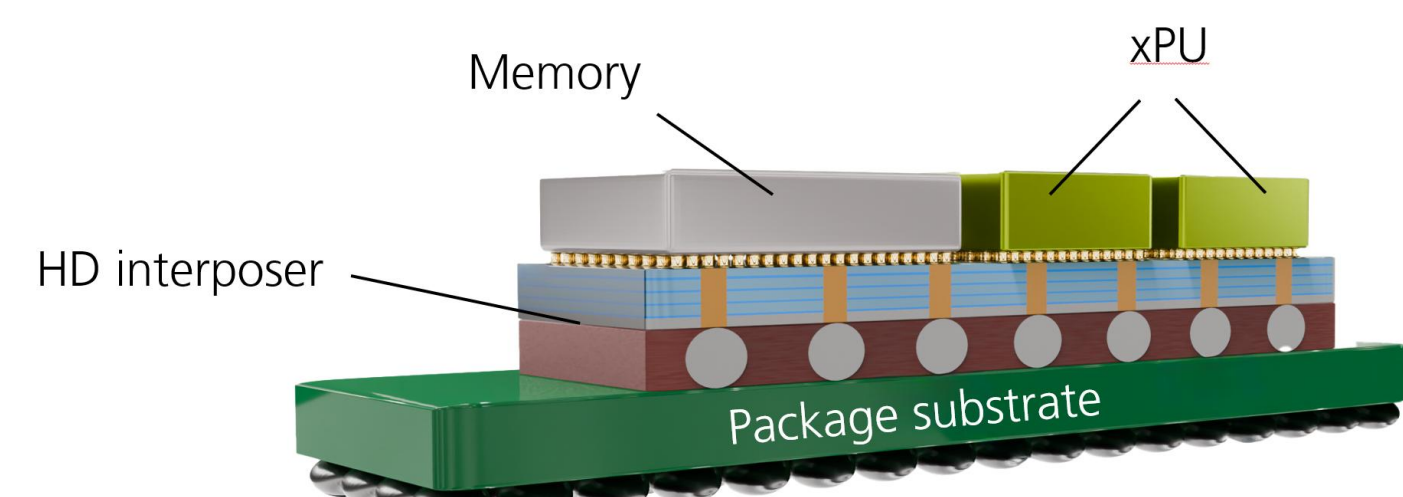
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Overview

During the start-up of the APECS Pilot Line, four application areas of advanced heterogeneous integration are addressed by the realization of demonstrators that highlight and evaluate the combined capabilities of the pan-European project partners: High Performance Computing (HPC), Multi Material Sensor (MMS), Optical Transmitter, and Radio Frequency Solutions. The chosen APECS demonstrators validate the pilot line operation by utilization of the conceived decentralized design and process capabilities (STCO). In particular the logistical and technological interfaces between different cleanrooms of varying requirements and the efforts needed to enable designers to use the different technologies. The aim is not only to optimize the transfer between processing steps, but also to enable process combinations that expand the capabilities of chiplet technologies and hetero integration alike while maintaining efficiency close to a centralized process environment. The resulting demonstrators were chosen to address most current challenges in microelectronics and yield chiplets ready for integration or chiplet modules.

High Performance Computing (HPC)

Demo 1 - High Performance Computing

The HPC demonstrator of the APECS project shows how high bandwidth data transfer requirements of high-performance computing can be tackled according to different needs for different applications. For the scalability of those systems, it is very advantageous to have separate chiplets for peripheral communication and for computing to adapt the system in short time by the kind and number of chiplets. Also to address the demands on interfacing change in a different time scale different compute chiplets will be the solution. Furthermore, the decision to have memory inside or beside the compute chiplets shapes the systems in terms of power consumption and ability, not only to be able to compute on streams, but also on larger chunks of data at a time.
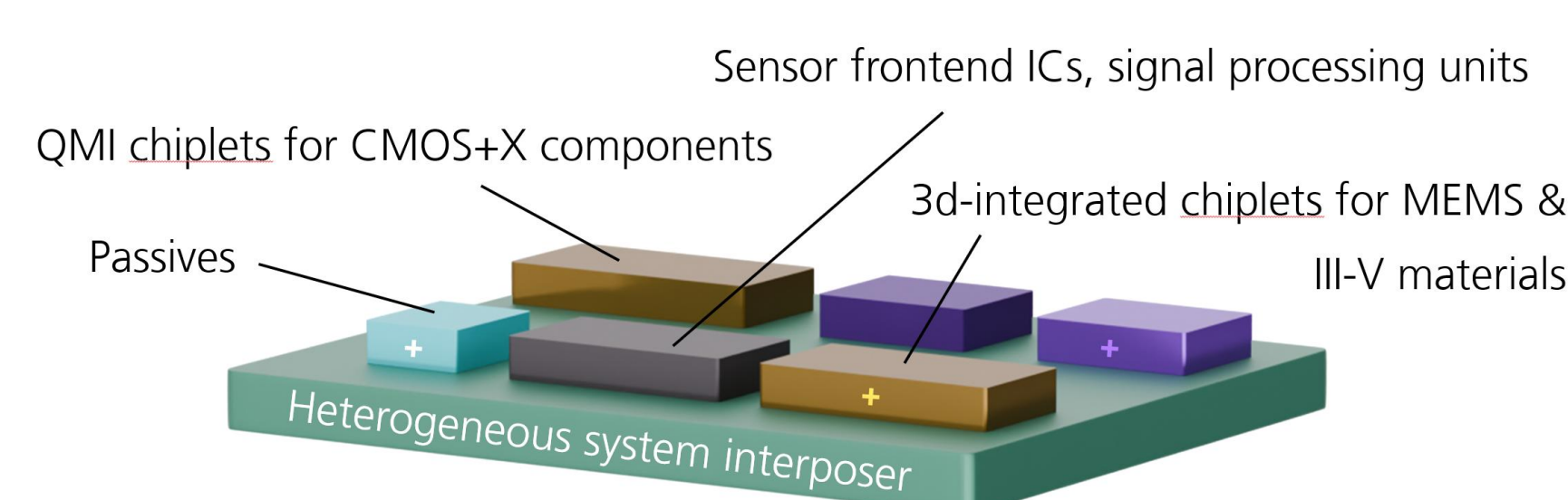
Two functional and several non-functional HPC demonstrators will set examples of a more versatile heterogenous integration than it is currently available to address key challenges in the European electronics market. One functional demonstrator implements a high performance computing unit for data center, the other an ultra low power mixed-signal AI chiplet module for mobile AI based systems with RF interface.

There will be the manufacturing of ultra-high-density redistribution layers and through silicon vias. Also, resistors and capacitors will be embedded into silicon interposers. The work package will furthermore improve assembly on advanced organic substrate.

Within the APECS pilot line development the HPC demonstrator will not only show the capability of the line itself but also the advantages of System-Technology-Co-Optimization (STCO). A customized set of PDKs and ADKs will be generated, used and evaluated. The demonstrators will also help to find a common language between the worlds of system and technology to provide the technology to a wider audience.

Multi-Material Sensor (MMS)
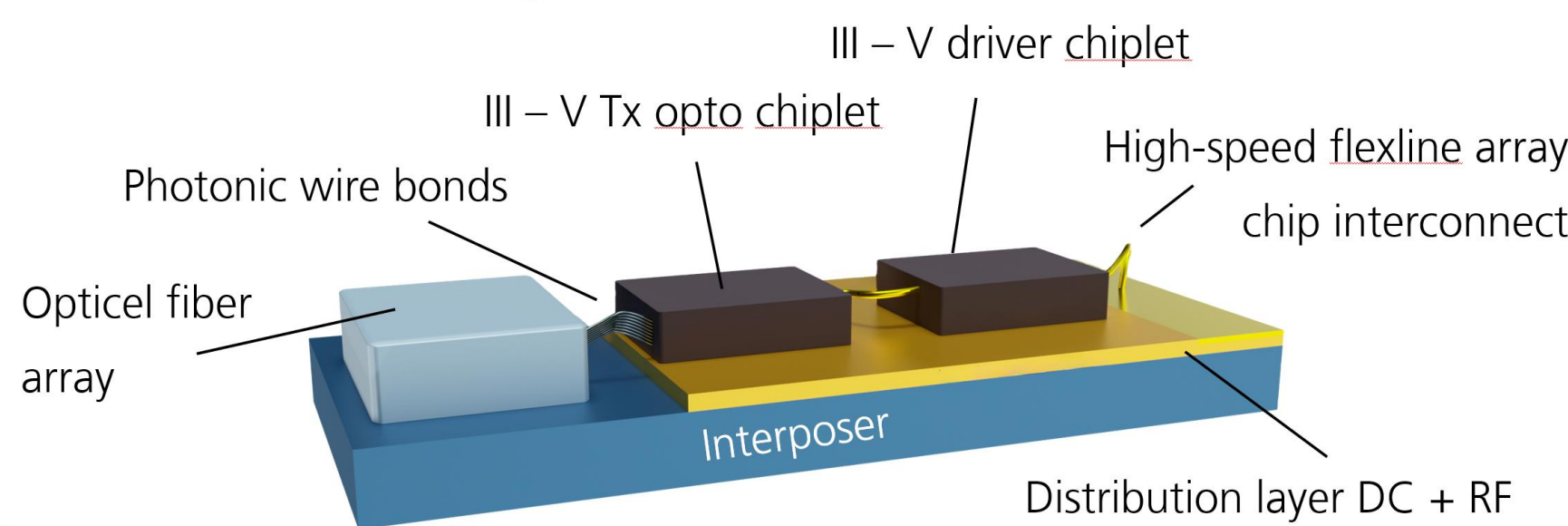

Demo 2 - Multi-Materials Sensors

Semiconductor sensor systems are becoming increasingly complex and highly specialized based on the sensing modality. As such each type of sensor has unique integration and packaging challenges. Additionally, for most modern sensors an increasingly level of in sensor data processing is desired to increase the overall system efficiency, reduce communication bandwidths and partition system components. These challenges are addressed in the Multi-Material Sensor (MMS) demonstrator (see Figure) that pushes current heterogeneous processing and integration capabilities by combining MMS-chiplets with heterogeneous system interposers and advanced sensor frontends (digital and mixed-signal). The latter can be augmented with additive neuromorphic accelerators for utmost energy efficiency and latency.

Based on an initial sensor chiplet technology selection among the APECS partners, a diverse set of application domains with their unique technological emphases has been chosen to be addressed in this demonstrator – namely optical, gas, magnetic field and acoustic sensing.

Following the distributed pilot line approach and a common STCO approach among all application areas, discrete processing and integration value chains are realized within APECS. The resulting IP portfolio shall offer design flexibility and fast development times for different applications. The processing steps are selected to be scalable for pilot series production. As such, the different combinations of components compose a versatile and generic approach towards end-to-end design flows and methodologies for chiplet-based advanced heterogeneous system integration.
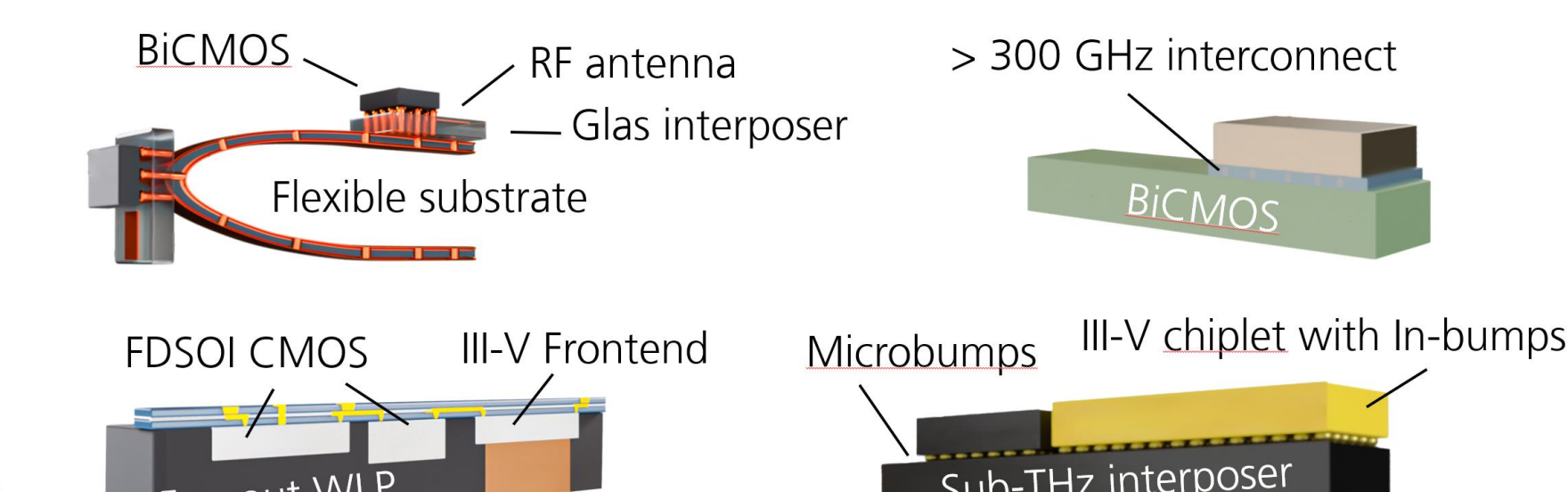
Optical Transmitter for HPC

Demo 3 - Photonic Systems

For this demonstrator an InP EML array chiplet will be integrated with an InP-HBT EML driver chiplet on a common interposer and coupled to an optical fiber array. The electrical high-speed connection between EML 4-array and driver uses polymer-based RF flexlines. Therefore, the photonic integration pilot line capabilities will be proved with a hybrid integration of InP chiplets on an interposer with photonic wire bonds (PWB) for the optical fiber coupling to a glass-based connector. A hybrid integrated high shoreline density o-band 4 channel transmitter (4x200Gb/s) for I/O in HPC systems will be realized.

Radio Frequency Solutions

Demo 4 - Modules for Radar and Mobile Communication

In the area of complex, highly integrated RF systems, four different technology demonstrators will be used to show the performance and innovative power of the various combinations of semiconductor and heterogeneous integration technologies. The fields of application that can be addressed from the latest generation of mobile radio applications and wireless links to radar applications. The focus is also on the practical testing of the design enablement developed in APECS (ADKs, tools, etc.) as well as metrological verification and series testing.

Conclusion

The demonstrators in APECS will show the seamless cooperation of 15 institutes within the pilot line. Nearly all hetero integration technologies will be implemented in a final set of seven independent modules. These will address core tasks in microelectronics, such as high-performance computing, modular sensor technology, data and telecommunications, and radar technology. Beyond the technological approaches, the principle of system technology co-optimization (STCO) will help to respond quickly and in a resource-efficient manner to the requirements of industry.

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Additional information

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