Picosecond Pulse Generation Methods for Die-to-Die ESD Testing

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***Abstract*—Due to miniaturization and heterogeneous integration of chiplets in the semiconductor industry, a need for electrostatic discharge (ESD) testing of die-to-die (D2D) interfaces has emerged. Current ESD testing methods, such as transmission line pulsing with switching relays, cannot reliably replicate fast D2D ESD events. Hence, novel pulse generation schemes reducing the transition time to below 50 ps are required. This work presents two methods of picosecond pulse generation with broadband radio-frequency amplification for D2D ESD testing. A high-speed arbitrary waveform generator is leveraged to generate short pulses achieving transition times down to 6.4 ps and amplitudes up to 28 V after amplification. Pulse generation with step recovery diodes yields transition times below 30 ps and amplitudes up to 19 V after amplification. While pulse generation with step recovery diodes is simple, less costly, and yet effective, the approach using high-speed arbitrary waveform generation shows overall better results. The presented pulse generation methods can be applied to future ESD testing of D2D interfaces in heterogeneously integrated devices.**

***Index Terms*—Advanced packaging, electrostatic discharge (ESD), heterogeneous integration, picosecond pulse generation, transmission line pulse (TLP).**

I. Introduction

Hetero-integrated device technology, often also denoted as advanced packaging, has been a growing trend in the semiconductor research and industry. Advanced packages connect multiple bare dies (chiplets) to each other before packaging, e.g., using through-silicon vias in die-to-die (D2D), die-to-wafer, or wafer-to-wafer bonding. Electrostatic discharge (ESD) events may occur during the processing, e.g., placement in pick-and-place machines or while performing D2D connections of these chiplets, which lead to failure [1–4]. Recent studies have shown that due to the miniaturization of the chiplets in advanced packaging, the voltage level and pulse duration of an ESD event are both reduced [2–4]. Hence, the industry is proposing lower target voltages from 3 V up to 30 V for D2D ESD testing [5, 6]. The pulse duration of D2D ESD events ranges in the low hundreds of picoseconds, while the transition times are sharpened to tens of picoseconds [3, 4]. Further, conventional field-induced charged device model (CDM) testers do not reproduce well, especially at low pre-charge voltages and are limited in their measurement bandwidth [2]. Methods such as capacitively coupled transmission line pulse (CC-TLP) and low-impedance contact CDM have been proposed for future D2D ESD testing [3, 4]. Studies in ESD testing of high-speed integrated circuits have shown that the transition time influences the ESD failure threshold [7, 8]. Hence, transition times $\leq$50 ps are of interest for further studies [7, 9].

Current TLP generator technology has primarily focused on switching relays, achieving voltages $\geq$100 V, pulse widths $\geq$1 ns, and transition times $\geq$100 ps. Due to the reduced transition times observed during D2D ESD events, the bandwidth for measurement and ESD testing must increase accordingly [7, 10]. This work proposes pulse generation schemes and prototypes for low voltage and short transition times for D2D ESD testing. Radio-frequency (RF) pulse generation schemes are leveraged to generate short ESD pulses with fast transition times requiring a high bandwidth. Transition times in the range of 7 ps to 60 ps and voltage levels up to 18 V are achieved. The pulse generation schemes may be used as high-bandwidth pulse sources for ultra-fast TLP or CC-TLP.

The presented work is structured in the following order. Fundamental background information is given in Section II. Further, Section III introduces a pulse generation concept with an arbitrary waveform generator (AWG) and broadband amplification. An alternative concept relying on step recovery diodes is discussed in Section IV. A conclusion and an outlook to possible further research is given in Section V.

II. Background

To avoid ESD damage of semiconductor devices (dies, chips), protection components, such as diodes and transistors, are built within the device. These protection components then divert ESD currents, e.g., from an input/output pin to ground. To verify these protection components, ESD testing is performed. ESD testing aims to identify which type of ESD can be handled and to what extent, i.e., the maximum ESD voltage or current. Hence, ESD testing methods aim to replicate known ESD events to determine when a failure is reached. The human body model (HBM) and the charged device model (CDM) are common models to characterize ESD events. Corresponding HBM and CDM (device level) ESD testing standards have been developed for industrial use. TLP standards for ESD testing have also been introduced and

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require pulse sources. TLP tests leverage pulses with transition times of double-digit nanoseconds. The adapted very-fast TLP (vf-TLP) and CC-TLP standards reduce the transition time down to 100 ps [11]. ESD testing standards requiring lower transition times have not yet been published, to the best of the author's knowledge. Moreover, in vf-TLP and cc-TLP testing, the difference between the incident and reflected pulses can be used to analyze underlying ESD structures and identify ESD failures.

The discharge waveform of an ESD event can vary depending on multiple factors, including the exposed die or chip [2]. D2D bonding is typically performed by the manufacturer in controlled environments; therefore, these interfaces are not at significant risk of ESD damage once fully packaged [3, 4]. Further, ESD prevention devices such as air ionizers also limit the charging of chiplets during processing [2]. Hence, the expected discharge amplitudes are reduced, as are the test levels [5]. Further, the short distances of D2D interconnects result in very little inductance. This leads to a short pulse duration and reduced transition times [2].

In [3], single-digit picosecond transition times and pulse widths around 200 ps were observed in a laboratory pick-and-place setup. Continuing studies in [12] showed transition times between 15 ps and 195 ps with most of them $\leq$50 ps. Observed pulse duration, measured as full width at half maximum, averaged between 55 ps to 87 ps [12]. Measurements and simulations in [4] showed transition times mainly between 30 ps and 65 ps, with some outliers $\leq$30 ps. As pulse duration, determined by the first ringing period, values from 200 ps to 500 ps were observed [4]. Circuit and full-wave simulations in [2] resulted in double-digit picosecond transition times and pulse widths. The previously stated studies show shorter pulse durations and transition times for smaller chiplets.

The transition time and frequency bandwidth of linear time-invariant systems are inversely related [13]. For a first-order low-pass the relationship between transition time (t_t, 20% to 80%) and the frequency bandwidth (f_b, 3 dB) is

$$t_\mathrm{t} \approx \frac{0.22}{f_\mathrm{b}}. \tag{1}$$

For digital baseband signals, a similar inverse relation can be drawn between the pulse duration and the required frequency bandwidth. Therefore, future TLP testing, e.g., for CC-TLP or ultra-fast TLP, pulse sources with transition times as stated above must support greater bandwidths, e.g., up to 20 GHz.

III. AWG Pulse Generation

Reproducible and modular pulses can be created with digital-to-analog converters (DACs). An AWG contains a DAC, which feeds a low-pass filter (LP) and an output stage amplifier (AMP) as seen in Fig. 1. Within the proposed setup, a short pulse is generated by a high-speed AWG (Keysight M8195A) and then amplified with an RF-amplifier (RF-Lambda RAMP01G31GD, denoted RF-AMP) as seen in Fig. 2. In order to avoid overdrive and protect the inputs of the RF-AMP and the oscilloscope (Scope), additional attenuators

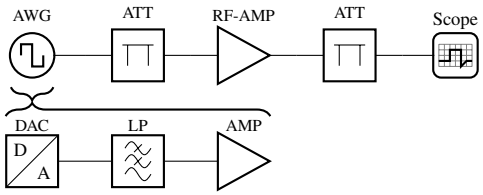


Fig. 1. Pulse generation measurement schematic with high-speed AWG.

Fig. 2. Digital pulse generation for a compromised pulse with reduced leading undershoot.

(ATT) were placed in between. Here, the bandwidth of the AWG is rated for 25 GHz with up to 65 GSa/s and the RF-AMP has an operating frequency range from 0.2 GHz to 35 GHz. The oscilloscope (Keysight UXR0702B) has a maximum bandwidth of 70 GHz with up to 256 GSa/s while the attenuators range up to 40 GHz.

The uneven frequency response and non-linearity of the RF-AMP distort the pulse as seen in Fig. 4. The measured rise time of the positive pulse is at 25 ps (green $\star$). The fall time of the negative pulse in Fig. 5 is 21 ps. The positive and negative pulses exhibit further differences beyond their polarity due to the non-symmetry of the RF-AMP. The transition time can be improved with digital predistortion of the pulse, including frequency responses of the RF-AMP, cables, and AWG. The frequency response of the AWG is provided by the manufacturer and is shown up to 31 GHz in Fig. 3. Further frequency responses were measured with a vector network analyzer (Keysight N5227B) and combined into a single two-port (green $\star$). The rise time can be improved down to 6.4 ps but causes a leading undershoot (orange $+$, Fig.4). The fall time was improved to 8.4 ps.

In some cases, a leading under-/overshoot may be unwanted to avoid any pre-stress on the tested components before the actual sharp pulse is sent. In order to reduce the leading under-/overshoot the pulse waveforms of the original pulse and the predistorted pulse are combined as seen in Fig. 6. For $a = 0.5$, a compromise between minimal transition time and pulse shape (blue, Figs. 4 & 5) can be achieved, resulting in a rise and fall time of 8.5 ps and 10.3 ps respectively.

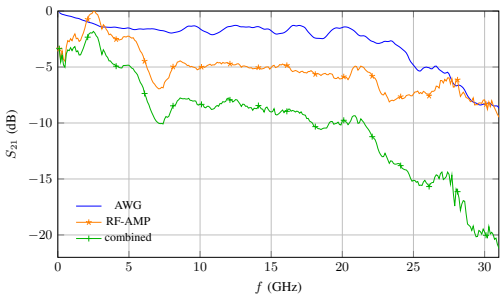
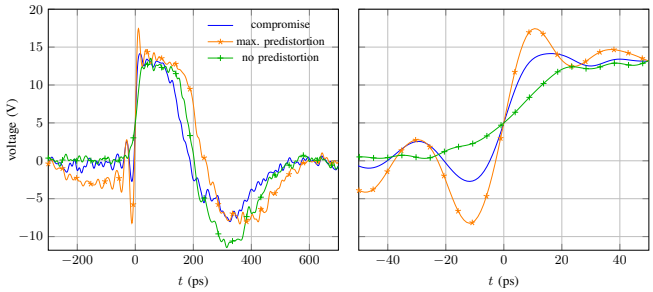


Fig. 3. Frequency response spectrum for AWG, RF-AMP, and both combined with cables. Extrapolated to DC and normalized to the maximum.

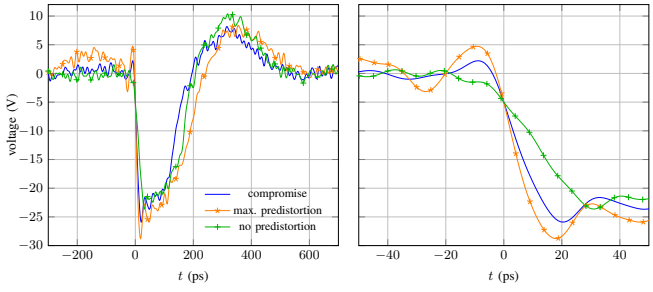


(a) Full pulse. (b) Rising edge.

Fig. 4. Measured amplified high-speed AWG positive polarity pulses. No predistortion in green ($\star$), fully predistorted in orange ($+$), and a compromise in blue ($a = 0.5$).

Due to the short pulse duration, no settled top level can be determined, hence the rise time was measured between 0 V and the pulse maximum while using 20% and 80% as thresholds. The presented predistorted pulses measured transition times with a standard deviation of $\leq$600 fs. Compared to switching relays which are prone to deviate in their performance from pulse to pulse, the presented pulses are highly reproducible.

The maximum voltage achieved for the positive pulse is 18 V. Due to the non-symmetry of the RF-AMP, especially when approaching saturation, the negative pulse can reach up to −28.8 V. When setting $a = 0.5$ the positive and negative pulse reach 14.9 V and −26 V, respectively. The more high-frequency components the pulse contains via predistortion, the



(a) Full pulse. (b) Falling edge.

Fig. 5. Measured amplified high-speed AWG negative polarity pulses. No predistortion in green ($\star$), fully predistorted in orange ($+$), and a compromise in blue ($a = 0.5$).

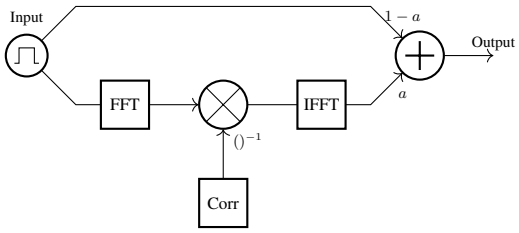


Fig. 6. Pulse predistortion block diagram.

shorter the transition time and the higher the maximum of the pulse. Lower amplitude pulses may be generated digitally or through analog attenuation. There would be the following options (compare Fig. 1):

- Reducing the gain of the AWG output stage (AMP)
- Reducing the bit range of the AWG
- Analog attenuation prior RF-AMP
- Analog attenuation after RF-AMP
- Reducing the gain of the RF-AMP

Here, the gain of the RF-AMP was not adjustable. Analog attenuation may only have coarse granularity compared to steering the AWG. However, reducing the bit range would result in quantization noise. A reduction of noise may be achieved by combining the differential output of the AWG with a broadband balun. Longer transition times can be set digitally or by adding low-pass filters.

IV. SRD Pulse Generation

Sub-nanosecond pulses can also be generated with step recovery diodes (SRD) and have been used in communication applications such as ultra-wideband [14]. Compared to the high-speed AWG approach, SRDs can act as frequency multiplier and therefore only require a low-frequency trigger source. This could reduce the cost for a pulse generator. Often, also nonlinear transmission lines (NLTLs) are leveraged to reduce the transition time to less than 10 ps [14]. NLTLs limit the voltage of the pulse due to the diodes within the NLTLs. To overcome the voltage limitation of single-digit volts, the use of broadband RF-amplifiers is proposed. Figs. 7 & 8 show the adapted setup where the high-speed AWG is replaced by an SRD pulse generator (SRD Gen), comprising two SRDs and a low-frequency trigger source (Trig Src) which outputs much longer transition times. To switch the polarity of the pulses, generated via the pair of SRDs, the orientation of both diodes and the polarity of the trigger signal are inverted.

A. Simple SRD Pulse Generation

Here, an AWG (Zurich Instruments HDAWG) with a bandwidth of 750 MHz and a sample rate of 2.4 GSa/s is used as a trigger source and Microchip GC2510 SRDs. As a trigger signal, a single sine period with a frequency of 100 MHz is used. For a positive pulse a 180° phase shift is set as seen in Fig. 9a. The output of the two SRDs, prior amplification can be seen in Fig. 9b. Fig. 10 shows the measured SRD-generated and amplified pulses. The positive pulse peaks at 12 V with a

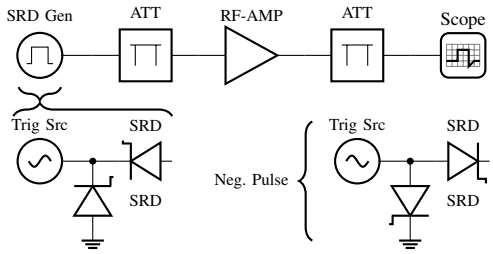


Fig. 7. Pulse generation measurement schematic with SRDs for positive pulses. Negative pulse generation with SRDs on the bottom right.

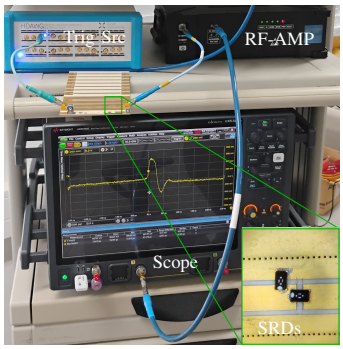
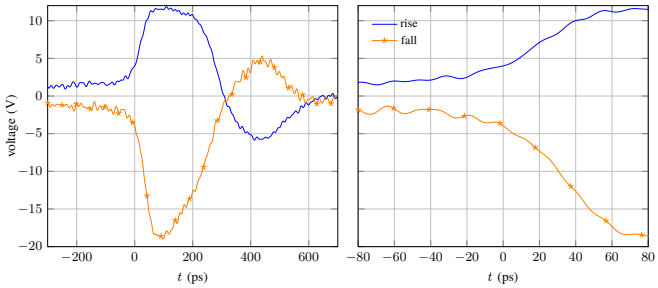


Fig. 8. Pulse generation measurement setup with SRDs and low-speed AWG as trigger source.



(a) Full pulse. (b) Edge.

Fig. 10. Measured amplified SRD generated pulse with trigger signal and SRD output from Fig. 9. Rise time of 57.7 ps, fall time of 50 ps

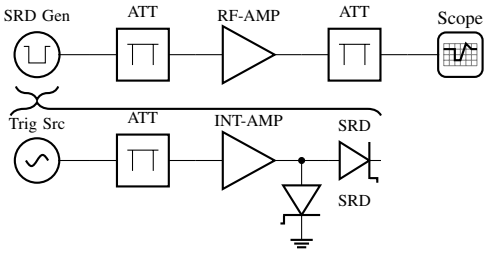


Fig. 11. Pulse generation measurement schematic for SRDs with improved transition time. Negative polarity pulses only.

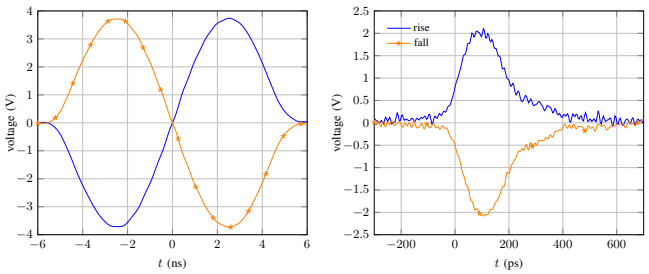
rise time of 57.7 ps. The negative pulse peaks at −19 V with a fall time of 50 ps. Due to amplifier distortion, the pulses exhibit a leading offset and a trailing under- or overshoot. As with the pulses above, the negative pulse shows a larger amplitude due to the non-symmetrical properties of the RF-AMP. Here, no digital predistortion is possible to adjust the pulse shape. Further, the RF-AMP cannot be overdriven as effectively as with the high-speed AWG setup. Therefore, the maximum pulse amplitude is lower.

B. Improved SRD Pulse Generation

In order to improve the transition time to $\leq$ 50 ps, fast-switching SRDs (MACOM MMDB30) are used. Further, the low-frequency trigger signal was increased in frequency and voltage to generate short pulses. Fig. 11 shows the adjusted measurement setup. The same trigger source is used but amplified with an intermediate amplifier (INT-AMP) due to amplitude limitations. Additional attenuation was inserted to avoid any overdrive. The measurement setup is shown in Fig. 12.

As above, single period sine waves are used as trigger signals and can be seen in Fig. 13a. A negative sine wave was used for a negative pulse due to the inverted output of the INT-AMP (SHF75P). To reach shorter transition times, the sine wave frequency was set to 200 MHz and 400 MHz. The output of the pair of SRDs is shown in Fig. 13b.

Fig.14 shows the final RF-amplified pulses for both 200 MHz and 400 MHz trigger signals. A maximum amplitude of −18 V and −19.2 V was achieved for 200 MHz and 400 MHz respectively. The transition time was improved from



(a) Trig Src. (b) SRD output.

Fig. 9. Measured trigger signal (b) and SRD generated pulse prior to amplification (b).

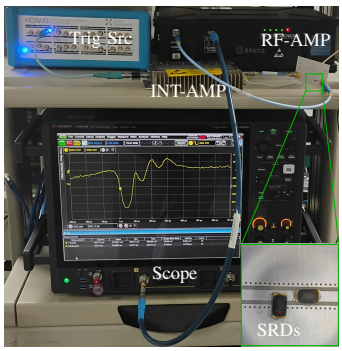
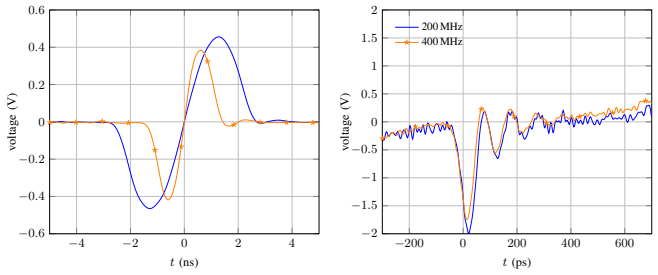
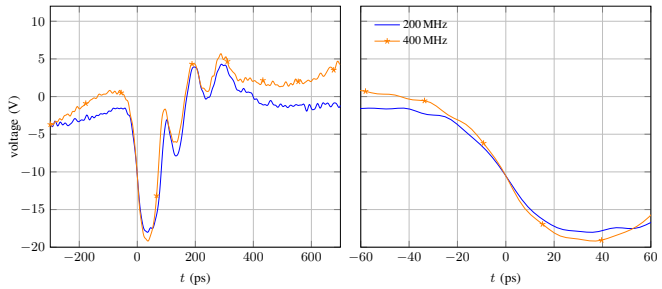


Fig. 12. Pulse generation measurement setup with SRDs for improved transition time, including an intermediate amplifier.



(a) Trig Src. (b) SRD output.

Fig. 13. Measured trigger signal (b) and SRD generated pulse prior to amplification (b).



(a) Full pulse. (b) Edge.

Fig. 14. Measured amplified SRD generated pulse with trigger signal and SRD output from Fig. 14. Fall time of 29.8 ps and 25.5 ps for tigger frequencies of 200 MHz and 400 MHz respecitvely.

29.8 ps to 25.5 ps by doubling the trigger signal frequency. However, leading and trailing distortion increased as well. The presented pulses measured fall times with a standard deviation of $\leq$1.2 ps, showing high reproducibility. Also, positive pulses were created by switching the polarity of the SRDs. Amplitudes of up to 12.4 V and rise times down to 26.5 ps were achieved.

Compared to the high-speed AWG approach, the SRD pulse generation shows slower transition times and reduced amplitudes. Further, the pulses are more distorted as no digital predistortion can be applied. However, the SRD pulse generation setup would be less costly compared to a high-speed AWG and achieves transition times which were observed in previous studies (see Sec. II). Furthermore, results in Fig. 14a showed narrow pulse widths (full width at half maximum) $\leq$100 ps.

Using SRDs, lower pulse amplitude voltages could be achieved by reducing the amplitude of the trigger signal or reducing the gain of the INT-AMP. However, this only works up to a certain extent, as the switching behaviour of the SRDs is highly non-linear. Hence, analog attenuation may be preferred. Further improvement on the pulse shape, i.e., the transition time, may be achieved via the usage of an RF-equalizer. An RF-equalizer could flatten the frequency response of the RF-AMP and connecting cables (see Fig. 3).

V. Conclusion

This work presents two pulse generation options for D2D ESD testing. The proposed pulse generation may be used in ultra-fast TLP and CC-TLP setups to characterize RF-chiplets or advanced packages with D2D interfaces. A high-speed AWG or a pair of SRDs were leveraged for pulse generation and amplified with a broadband RF-amplifier. Transition times down to 6.4 ps and amplitudes up to 18 V and −28.8 V were achieved with the high-speed AWG approach. The SRD approach yields transition times down to 25.5 ps with an amplitude of −19.2 V. Pulse generation via the high-speed AWG shows multiple advantages, as the pulse form is much more tunable than with SRDs. However, SRD pulse generation is simple to implement and can reduce cost. In general, a trade-off was observed between reduced transition time and increased distortions for both approaches.

Future work may improve the transition time, pulse shape, and pulse amplitude to better match real-world D2D ESD events. Furthermore, ESD stress testing, e.g., by using CC-TLP, with the proposed pulses must be analyzed and correlated to ESD protection device failures observed in the field.

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