Characterization, testing & reliability for heterogeneous integration of chiplets

Daniel Kriesten, Fraunhofer ENAS, Chemnitz, Germany, daniel.kriesten@enas.fraunhofer.de
Norbert Pöllmann, Fraunhofer ENAS, Chemnitz, Germany, norbert.poellmann@enas.fraunhofer.de
Julia Wecker, Fraunhofer ENAS, Chemnitz, Germany, julia.wecker@enas.fraunhofer.de
Dominik Schröder, Fraunhofer ENAS, Paderborn, Germany, dominik.schroeder@enas.fraunhofer.de
Sebastian Brand, Fraunhofer IMWS, Halle, Germany, Sebastian.brand@imws.fraunhofer.de
Christopher Benndorf, Fraunhofer IMWS, Halle, Germany, Christopher.benndorf@imws.fraunhofer.de
Emanuele Strieter, Fraunhofer AISEC, Garching b. München, Germany, emanuele.strieter@aisec.fraunhofer.de
Nisha Jacob Kabakci, Fraunhofer AISEC, Garching b. München, Germany, nisha.jacob@aisec.fraunhofer.de
Steffen Kurth, Fraunhofer ENAS, Chemnitz, Germany, steffen.kurth@enas.fraunhofer.de
Frank Altmann, Fraunhofer IMWS, Halle, Germany, frank.altmann@imws.fraunhofer.de

Abstract

The characterization, test and reliability methodology for advanced packaging and heterogeneous integration of electronic components and systems is requesting a holistic approach that combines characterization and testing as well as key innovation to ensure safety and functional reliability. The modular nature of such systems with the wide variety of signal types, amplitudes and frequencies, and with the high integration density creates new topics for research and development. Novel concepts, methods and instrumentation will be developed to tackle these challenges as part of the fabrication pilot line APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems). The contribution shows technical concepts of particular set-ups, methods for characterization and test and for analysis of reliability issues as well as secure operation.

1 Introduction

Future microelectronic systems require more and more functionality of the modules. It cannot be achieved by the integration at a single chip using a dedicated semiconductor technology based on one substrate material (e.g. Si-CMOS, GaAs or other) in an economic manner. Instead, one of the trends is to fabricate chiplets with different requests on the specifications and function and to combine them by complex 2.5D or 3D integration technologies to achieve the desired performance of the overall system. It has been successfully followed by a number of semiconductor companies (e.g. Intel, TSMC, Sony, Samsung) [1]. Special functions, can be integrated into one system in package by using suitable optimal technologies based on related wafer material and manufacturing processes such as sensors, RF, mm-wave and sub-THz components and photonic components and interfaces as well as high-voltage components.

The applications of such complex and highly performing systems is not limited to high-speed computing and AI [2,3] but also expected in high-speed communication using the combination of InP technology [4], waveguide networks [5] and high-speed CMOS, in optical sensing [6, 7] and quantum technologies [8].

The European Commission and the national authorities established semiconductor fabrication pilot lines designed to bolster the European Union's semiconductor industry and enhance its technological sovereignty as part of the activities under the European Chips Act. The pilot line APECS as one of these pilot lines is focusing on the development of heterogeneous integration and advanced packaging technologies based on the chiplet approach, including the dedicated design, characterization, test and reliability assessment capabilities.

This paper is the result of the first activities within the APECS pilot line and will shortly explain the specific challenges of test, characterization and analysis of reliability and security issues in a first chapter. Further sections show examples of the mentioned techniques and cover electronics and photonics characterization and test and methods for the analysis of electromagnetic field interactions, analysis of failures in packaging and how security issues can be detected.

2 Specific challenges

Heterogeneous integration of chiplets introduces more severe challenges than has been the case with conventional systems to date due to substantially narrower pitch of the interconnects, different signals in type, amplitude and frequency (DC, high speed, µ-wave, mm-wave, high power, optical). Moreover, the reliability is affected by a number of features as like as TSV related stresses, solder-based joints, underfill, passivation and moisture ingress or electromigration [1]. This often requires completely new solutions and innovations in characterization, test and failure & hardware security analysis techniques addressing the high complexity of heterointegration combining different semiconductor technologies in 3-dimensional functional structures with ultra-high densely arranged interconnects, which could also combine very different electrical and optical signal types. The integrated test and alignment structures will be particularly necessary for photonic, hybrid bonds, RF or

sub-THz interconnects and optical interconnects integration, to ensure the functional reliability and service life of the components in the application.
In order to ensure a sufficient yield, efficient methods for burn-in tests and chiplet tests at wafer level become necessary to determine the "known good dies" for heterogeneous integrated systems.
As a result of new features of the 2.5D/3D integration technology (TSVs, high density interconnects, novel material combinations, hybrid bonding, CT mismatch of very tiny structures, high electric field strength, high current density), they may introduce new failure mechanisms and combination of failure mechanisms as well. It is expected that interlocking combination of electrical reliability testing and material characterization, including the provision of state-of-the-art defect analytics, failure diagnostics and virtual testing and modelling techniques become a key differentiating factor for the market success of future highly complex heterogeneous electronic systems. High-resolution, non-destructive 3D characterization and defect metrology for micrometer-scale assembly and joining technology based on micro-bumps, TSVs, TGVs and hybrid bonding need to be applied.
To complete the topic, a holistic approach to life cycle modelling (early failures, defects during operation, end of life) shall help to achieve a zero-defect rate that is scalable from the laboratory to production.
In the area of characterization and test, it is expected to develop advanced characterization tools and methods for materials, chiplets and QMI systems with large variety of signal types (DC, RF, high speed digital, mm-wave, sub-THz, optical) and to build high accurate and low-noise measurement capabilities for determination and evaluation of heterointegrated devices. Facilities for wafer-level and chip-level testing for optical, RF, and mm-wave signals, …80 Volt, … 18 GHz in the clean room and test heads for wafer level and chip level optical and RF/mm-wave tests for optical communication (device2device, interchip) will be established. They will be used for

- Characterization of high-speed transmitter and detector chiplets
- Efficient electrical characterization tools (high accurate, low noise)
- Electro-optical characterization of QMI systems with backend optics
- Antenna and RF component characterization from mm-wave to THz
- Characterization of high-performance optical interconnects

in order to measure

- Connection, maximum current
- Isolation, maximum voltage
- Impedance, signal integrity
- Electric circuit functionality
- Coupling loss (reflection, mismatch, scatter)
- S-parameters under load-pull
- Burn-in tests
- X-Ray in-line inspection.

In the area of reliability, failure and security analysis, reliability testing, capabilities for failure analysis and a framework to ensure hardware security along the manufacturing chain will be established. It aims to the implementation of architecture-level security measures and security IP blocks on chiplet, HI devices up to system level.
A comprehensive understanding of technology and application related defect risks and identification of new failure modes and degradation mechanisms is urgently necessary and need to consider the quality and reliability aspects during development aiming adequately improved designs for high reliability.

3 Characterization and Test: Congruence and complementarity

This chapter deals with the question of which test method or procedure should be used. The answer to this question ultimately has a major influence on the test system architecture and the associated costs.
The two possible procedures are: Wafer-Level Characterization and Testing to a Test Specification.
Wafer-level characterization and testing according to a test specification serve different purposes in the semiconductor development and manufacturing process.
Wafer-Level Characterization is primarily used during the early stages of process development and device validation. It involves detailed electrical measurements to understand the behavior and performance of a semiconductor device.
The goal is to extract device parameters (e.g., threshold voltage, leakage current, mobility) and analyse process variations, material properties, or design effects.
Characterization is often exploratory and may use flexible test setups and custom test routines. It typically targets a small number of test structures or dies and focuses on in-depth analysis rather than pass/fail decisions.
In contrast, testing to a test specification (often referred to as production testing or specification-based testing) is performed to verify that each device meets predefined performance criteria before it is shipped. These tests are derived from customer or product requirements and focus on identifying functional failures or out-of-spec parameters. The process is highly automated and standardized, ensuring each die is evaluated against the same limits. This testing ensures product quality, yield control, and compliance with datasheet specifications.
In summary:
Characterization: deep understanding of device behaviour; flexible, detailed analysis; used in R&D and early-stage development.
Test to specification: strict pass/fail criteria; automated and repeatable; used in high-volume production.
During the phase of technology development and for the fabrication of first prototypes by a pilot fabrication line, it was decided to use a “mixture” of both methods. On the one hand, this is a new technology, so we are at an early stage of process development. This means that characterization at wafer level would naturally be the preferred

method. However, to achieve secured results with statistical relevance, fast methods of specification tests need to be applied, and a certain degree of automation, as we know it from high-volume production, is therefore necessary.

4 Electric characterization and test of SiC diodes at wafer level

4.1 Test System Architecture

The following chapter describes the considered hardware architecture of the required wafer-level test cell for the ThinSiCPower project, taking into account the considerations made above.

The new wafer test system (Figure 1) consists of the following major parts,

- the Wafer Prober – required for fixing and positioning the wafer
- a Probe Card or Load Board – required for contacting the DUTs (the design depends on the chosen parallelism)
- the Tester – required for testing the DUTs
- and the adequate software – required for controlling the test cell

Figure 1: Power Wafer-Level Test Cell – major components.

All four parts result in the new wafer-level test system and each of these parts interacts with one or more of the other parts to perform their respective tasks.

4.2 Single-Site Wafer-Level Testing and Wafer Chuck

Single-site wafer-level testing (Figure 2) is a method used to evaluate the performance and integrity of individual dies directly on the wafer before dicing. In this testing approach as already said, only one die is tested at a time, allowing for more precise control of test conditions and higher accuracy in sensitive measurements. This method is particularly advantageous for devices with complex or high-precision analog and RF characteristics. Single-site wafer-level testing does not require a probe card, the die is contacted via fixed probe needles, which are attached to the prober head plate using suitable holders.

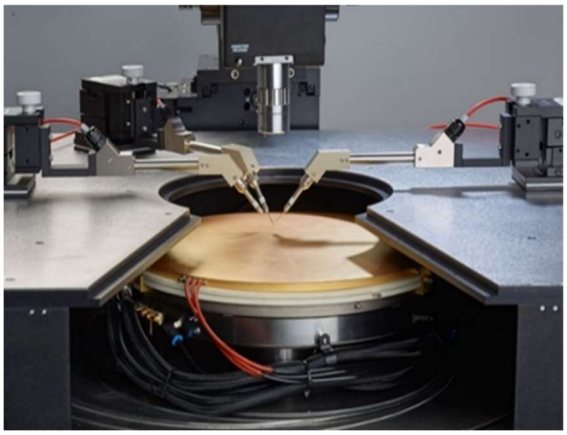

Figure 2: Typical measurement setup with test needles and holders for single-site testing.

A critical component in achieving accurate single-site measurements is the use of a triaxial chuck (Figure 3). Unlike standard chucks, a triaxial chuck offers enhanced electrical isolation and shielding by supporting three conductors: signal, guard, and ground. This configuration reduces leakage currents and minimizes noise, making it ideal for low-current and high-impedance testing. The guard connection, in particular, helps maintain a constant potential around the signal path, significantly improving measurement stability and repeatability.

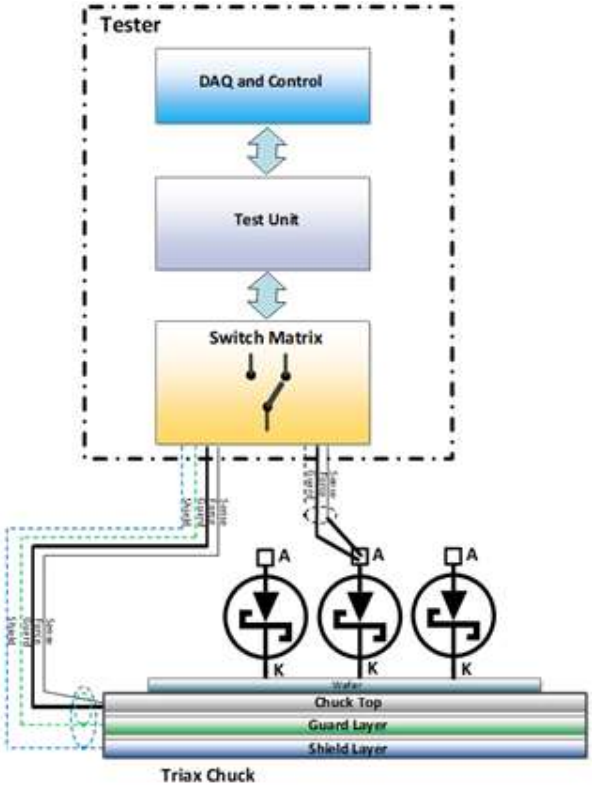

Figure 3: Schematic Diagram of the Wafer Test with a triaxial chuck and the connected ATE.

In practice, the combination of single-site testing and a triaxial chuck is commonly used in applications such as parametric testing, reliability verification, and testing of ultra-low leakage devices like sensors, MEMS, or advanced CMOS nodes. It allows engineers to detect subtle defects and process variations early in the manufacturing process, thus improving yield and reducing cost.
Overall, single-site wafer-level test using a triaxial chuck provides a robust solution for high-precision, low-noise semiconductor characterization at the wafer stage.

4.3 Test Program(s) and Definition of Test Parameters

It was decided together with the IISB to include the following test parameters in the test specification of the Schottky diode demonstrator.

- Repetitive Peak Reverse Voltage (VRRM)

VRRM is the maximum allowable repetitive peak reverse voltage of the diode in steady state and transient conditions before it suffers a breakdown. This breakdown limit is rated at an industry standard of 25°C temperature unless stated otherwise. It should also be noted that this breakdown limit might be reduced by approximately 10% at extremely low temperatures like -55°C.

- Diode Forward Voltage (VF)

VF is the diode's forward voltage drop specified as a function of the continuous forward current (IF) and junction temperature (Tj). The typical values of VF at different conditions of IF and Tj can be derived from the typical forward characteristics curve in the datasheet.
These values are specified for two temperatures, 25°C and 150°C. The pulse length of the current injected during this test is kept as minimum as possible to prevent discrepancy due to self heating.

- Reverse Current (IR)

IR is the reverse leakage current of the diode when a reverse voltage (VR) is applied across it. These values are specified at the rated DC blocking voltage at 25°C and 150°C. As electrons acquire higher energies at higher temperatures, it becomes easier for them to overcome the Schottky barrier, and therefore, leakage current increases with temperature.

5 Photonics

Even for photonic chipslets and systems containing optical signal transfer, automatic measurements conducted on a wafer prober will become necessary. A set-up using a wafer probe station has been developed and will be qualified and extended in the future (Figure 4). The wafer prober is equipped with a silicon photonics measurement system (FormFactor), which enables automated alignment of two optical fibers to the grating couplers at wafer level. Two tuneable lasers are used as light sources: a C-band laser (1528 nm – 1566 nm) from Quantifi Photonics and a white light laser (1100 nm – 2000 nm) from NKT Photonics. The white light laser with the tunable monochromators are used for characterizing of the broadband components since it provides a more complete representation DUT spectral behavior but with lower wavelength resolution. For characterizing of narrow band DUTs,, the resolution of the white light laser (line width approx. 8 nm) is not sufficient; therefore, the C-band laser, which achieves a resolution of 0.01 pm, is used. The transmitted power is measured with a power meter (Keysight).

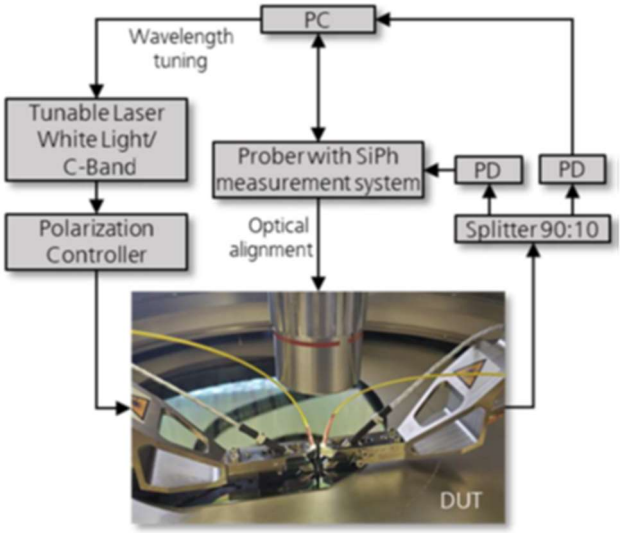

Figure 4: Measurement setup on wafer prober with two photode-tectors (PD) for optical alignment and measurement.

6 Near-Field Scanning for Electromagnetic Characterization and Testing

With the continuous miniaturization of integrated circuits such as chiplets and wafer-level integration, the demand for accurate electromagnetic (EM) characterization and testing at early development stages is steadily increasing. While 3D EM simulations provide valuable insight into the behaviour of simple structures, their applicability decreases for more complex geometries or broadband scenarios due to increasing model complexity and computational effort. In such cases, simulation accuracy is limited, or the computational effort becomes unfeasible. Therefore, physical measurements remain necessary for validating EM performance, characterizing field distributions, and identifying emission sources.

Near-field scanning (NFS) is a well-established method for the electromagnetic characterization of integrated circuits (ICs), components, and complete systems. Its traditional use cases include electromagnetic compatibility (EMC) characterization, antenna performance evaluation, and localized field mapping [9]. A advanced, high-performant NFS architecture that extends these capabilities to the wafer-level and chiplet-level, enabling non-invasive EM testing during prototyping and manufacturing, will be developed and established (Figure 5).

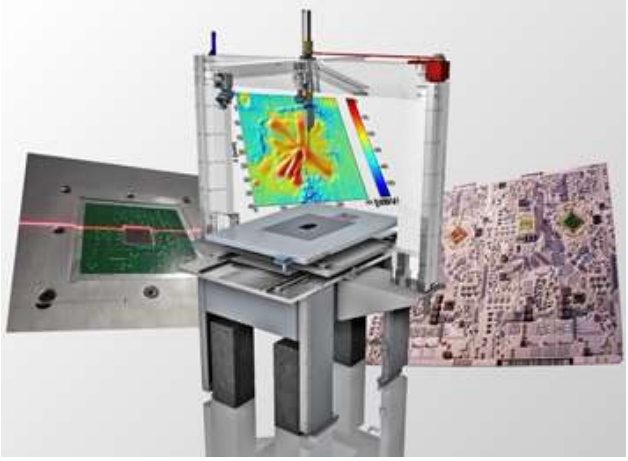

Figure 5: Model of the current near-field scanner along with a measurement result of an IC.

The system achieves a geometric resolution down to 1 µm moving around a changeable near-field probe in x,y and z-direction, including a rotational axis. Using two additional optical 3D-scanning units, the one to detect the NF-probe and the another to heightmap the device under test (DUT), enables a fully automated scanning procedure. This is reducing the effort for measurement setup and significantly accelerating the time-consuming scan process.
The scanner supports phase-resolved E-field and H-field measurements in all three spatial directions, with variable measurement distances ranging from several millimeters to a few hundred micrometers above the DUT. The measurement chain, consisting of a vector-signal-analyzer, frequency extenders, signal generators and LNAs covers a broad frequency range from kilohertz up to 100 GHz and beyond, depending on the selected probe and receiver hardware.
To enhance spatial accuracy, smart deconvolution techniques are applied during post-processing in order to correct for probe-specific transfer functions which may distort the measurements. This is improving both spatial resolution and quantity of the measured field values. This aspect becomes ever more important, the smaller the structures are and the closer to the source the measurement is performed [10]. Moreover, the resulting data serves as a basis for both source reconstruction algorithms and near-field to far-field transformations. The source reconstruction provides valuable insights into EM radiation mechanisms and assists the early design steps in the detection of EMC-critical structures or coupling paths. The derived near-field sources may also be used in 3D-simulations to evaluate the interaction within its intended environment [11]. Among many other applications, for example automotive radar sensor can be optimally placed in a car, or chiplets can be placed in low electromagnetic noise areas of interposers.

7 Failure analysis methods for 3D packages

For obtaining the required functional density and computational performance novel trends in microelectronics require dense integration of heterogeneous components in close proximity in all three spatial dimensions. Furthermore, such architectures need a electrical interconnection density at a small pitch to allow for direct communication, fast data transfer and lossless power supply. While these concepts open potential for innovation however, they highly challenge existing defect sensing and localization techniques particularly the once operating non-destructively. However, for ensuring the necessary reliability and robustness material behavior and interaction need to be understood in high detail, requiring failure analysis and metrology techniques. Prior to high resolution structural and chemical analyses, the potential deviation and evolving defects need to be reliably sensed and precisely localized, relying on non-destructively operating methods with microscopy resolution and sufficient sensitivity of an appropriate contrast mechanism. Non-destructivity is inevitably connected to inspection through layers of intermediate material which interact with the emitted waves or rays reflected or emitted from the sample's interior. When the structural complexity of the inspected specimen increases the interaction potential of the analysed waves increases, which leads to higher signal attenuation and signal falsification by e.g., interference effects. Non-destructively operating methods with microscopic resolution that are of high relevance in microelectronic metrology and failure analysis are e.g., acoustic microscopy (SAM), lock-in thermography (LIT), magnetic field and current path imaging (MCI) as well as x-ray inspection. SAM has a superior sensitivity to structural defects that involve different materials like cracks, delamination, inclusions and voids, however, is limited in resolution through the wavelength. Here increasing frequency only partially poses a solution as attenuation increases exponentially with frequency. A combined opto-acoustic approach will enable acoustic excitation inside the sample itself at the structure under investigation and may allow high resolution analysis of hybrid bonded interfaces. Lock-in thermography is highly sensitive towards temperature gradients. Through the lock-in approach it reaches sensitivities down to the µK-range and it thus a method sophisticated for the localization of heat accompanying electrical defects buried inside a complex heterogeneous sample. Here, the diffusive character of the heat propagation results in thermal spreading compromising the lateral resolution for localization of the thermal source. A novel phase sensitive approach will be employed to compensate the thermal spreading and enabling a real 3D-defect localization. Other methods that require sample preparation to some extent, leave the active structures functional for investigation at high resolution like E-beam probing, EBIC or EBAC also have their justification and are exploited towards their applicability for heterogeneously integrated complex microelectronic systems.

Due to challenges posed to fault diagnostics by the extremely small and complex structures in hybrid bonded systems, it is essential to combine various analytical methods in a synergistic way. Among these, imaging techniques of transmission electron microscopy (HRTEM and STEM) are particularly important, as they allow structural insights down to the atomic level. The use of EDX spectroscopy is considered a routinely applied method for chemical analysis; however, it shows significant limitations in terms of performance when applied to complex and small-scaled microsystems, including relatively high detection limits, quantification issues due to strong signal overlap, and strong absorption of low-energy X-rays by dense materials. Time-of-Flight secondary ion mass spectrometry (ToF-SIMS) offers an ideal solution to overcome these limitations. Extraordinarily high sensitivity with very low detection limits, high spatial resolution, and excellent mass resolution open the possibility to study hybrid bonded systems with a focus on structure, chemical composition, and the identification of sources of system failure. In recent investigations, the capability of the method was successfully used to characterize samples of wafer to wafer (w2w) and die-to-wafer (d2w) bonded systems (Figure 6). Very small structures, including Cu pads with diameters and pitches below 1 µm and layers of different dielectrics, can be clearly visualized to identify anomalies of the chemical composition indicating possible failure root causes. The high spatial resolution allows 'chemical' 3D sample imaging.

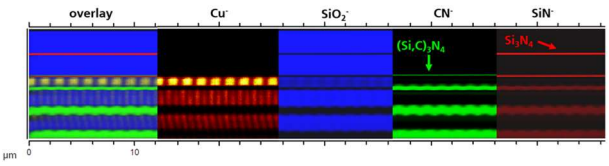

Figure 6: ToF-SIMS intensity profiles of the Cu-, SiO2-, CN- and SiN- signals obtained from a hybrid bonded w2w sam-ple with Cu pads (pitch under 1 µm) and layers of die-lectric materials with varying thickness shown in the x-z projection.

8 Hardware security of chiplets

Every chip production paradigm carries technology-based security risks. Chiplets are no exception to the rule. A cross-domain chiplet system can be thought of as a collection of diverse sub functionalities that work together while being flexible in addressing market demand. These sub functionalities can be developed modularly and produced by several parties in various technological nodes using diverse materials and combined on a single chip. Chiplets therefore promise to increase cost efficiency by optimizing wafer area, a more resistant supply chain using diversification with respect to production locations, while also enhancing scalability and yield allowing for a faster time-to-market. With the growing availability of such chiplets in the consumer domain, where most of those devices are physically accessible for adversaries, information security also plays a very important role. This means that powerful hardware-based attacks such as optical, side channel (SCA) and fault attacks (FA) pose a significant threat to all those devices.

Hardware security encompasses methods to keep electronic systems and devices safe from physical attacks, tampering and exploitation. This requires a thorough understanding of materials, architectural features, interconnects, electronic design, cryptography, signal processing, protocols and even supply chains.

Within the APECS pilotline project it is planned to establish security evaluation infrastructure for chiplets. This includes the creation of dedicated root-of-trust chiplet modules with post-quantum secure cryptography, state-of-art security testing methodologies down to research on common-criteria-like test-facilities allowing the pre-certification investigation of security relevant chiplet modules. The main topics of interest with regards to physical security analysis of chiplets are: chiplet preparation, localization of regions of interest or even whole chiplet modules of interest and finally the risk evaluation by analyzing and exploitation of design and production flaws in a trusted environment.

Physical security testing schemes like optical analysis and SCA require exposing the regions of interest on the die for further analysis. Newer packaging techniques that are common for modern System-on-Chips (SoCs) however pose a significant challenge as they stack dies or different chiplets within the same package thereby making chip preparation a major challenge during physical security testing of chiplets. Typical chip preparation schemes include mechanical thinning, chemical edging or even the transfer and re-bonding of chiplets for easy access. Due to diverse materials and integration complexity of chiplets, these classical preparations techniques need to be adapted for chiplets. Exposing the regions-of-interest improves localization methods to identify parts on the chiplet which are security related.

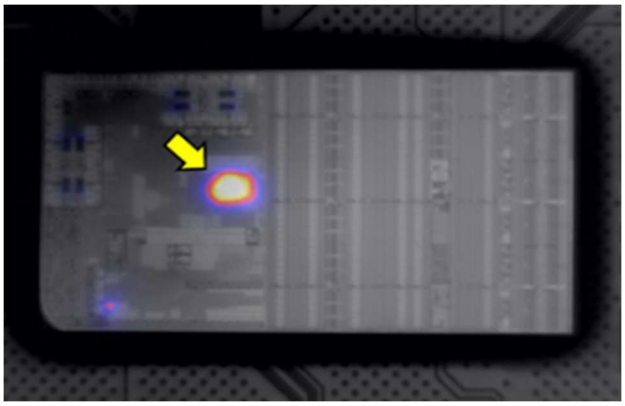

Figure 7: Example of a result of laser induced thermographic analysis of a Si chip

Optical analysis of ICs with methods like lock-in thermography, thermal laser stimulation, electro optical probing (or laser voltage probing) and photon emission measurements are essential tools in failure analysis of integrated circuits and have also been demonstrated to be powerful tools for

hardware security analyses. In the context of security analysis, these techniques can be applied to localize regions of interest for targeted security analysis and to extract secrets. Figure 7 shows a LIT evaluation of a complex System on Chip [12].

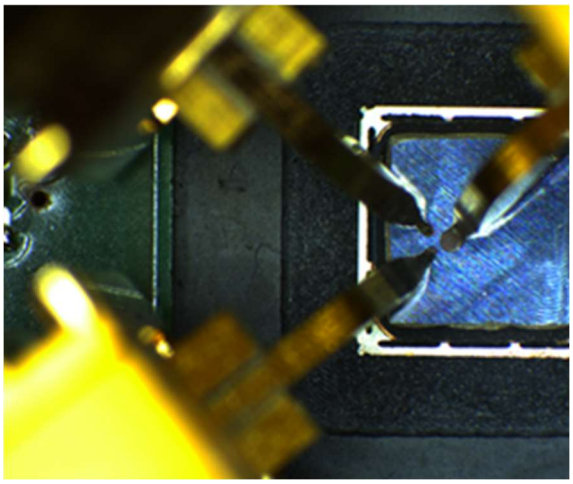

Figure 8: Top view of a chip with multiprobes for the analysis

Side-channel analysis is the backbone of security chip evaluations. The Power consumption or electromagnetic emanation of IC parts might leak information about intellectual properties or a secret value. APECS pilot line is a unique chance to understand the physical origin of leakages. It is planned to investigate advanced measurement methods like multiprobe and multi signal approaches, probing of on-chip buses and the exploitation of decoupling capacitors (Figure 8). The advanced measurement methods might be accompanied with more complex noise distributions and mass data. Classical as well as machine-learning based analysis methods will be used to focus on these challenges.

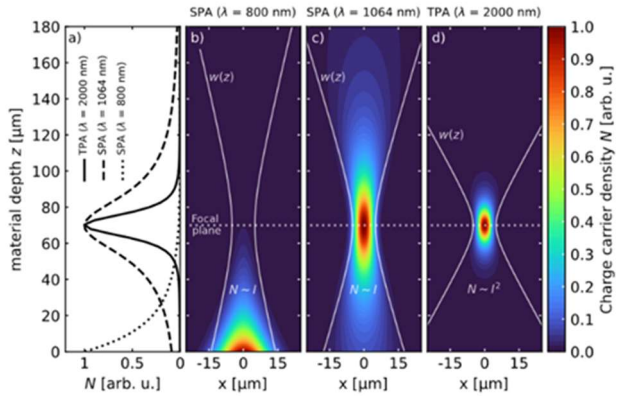

Figure 9: Theoretic prediction of the laser field intensity by laser fault injection with different wave length.

Fault injection attacks lead to computation errors within devices which are exploited to extract secret information, keys or to influence the execution flow for adversarial purposes. The most sophisticated and precise fault attacks are carried out by injecting current in electronic circuits using highly focused laser beams (Figure 9). These temporally and spatially precise lasers inject faulty values into one or more internal signals. State-of-art laser systems based on single photon absorption. The work in the APECS project will go beyond the state of art and will focus on developing a custom two-photon laser system, which might circumvent typical sensor-based fault injection sensors. Though two photon absorption is an established technique in other areas, e.g. fluorescence microscopy, so far it has not received much attention in the field of physical attack methods on integrated circuits. The APECS pilot line enables security research over the whole life cycle of chiplets.

9 Conclusions and future service offers

Novel integration technologies towards highly integrated systems with chiplets fabricated by different semiconductor technologies (heterogenous integration) requests appropriately qualified techniques for characterization test and analysis during the development phase and for fabrication by a pilot line or by volume production. The project APECS will tackle these issues by qualification and by new developments in the fields of electric, photonics and RF…mm-wave measurement and in the fields of failure analysis and analysis of hardware security issues.
APECS will provide the results as part of the pilot line together with requested chiplet and systems manufacturing and as a service for potential clients.

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