Advanced Packaging solutions for HPC, Communication and sensor modules enabled by APECS pilot line

Rafael Jordan[1], Elmar Herzer[2], Michael Mensing[3], Martin Möhrle[4], Henning Schröder[5], Marco Dietz[6], Michael Töpper[7]
[1]Forschungsfabrik Mikroelektronik Deutschland, Berlin Germany, rafael.jordan@mikroelektronik.fraunhofer.de
[2]Fraunhofer IIS, Erlangen and Dresden, Germany, elmar.herzer@iis.fraunhofer.de
[3]Fraunhofer ISIT, Itzehoe, Germany, michael.mensing@isit.fraunhofer.de
[4]Fraunhofer HHI, Berlin, Germany, martin.moehrle@hhi.fraunhofer.de
[4]Fraunhofer IZM, Berlin, Germany, henning.schroeder@izm.fraunhofer.de
[6]Fraunhofer EMFT, München, Germany, marco.dietz@emft.fraunhofer.de
[7]Forschungsfabrik Mikroelektronik Deutschland, Berlin Germany, michael.toepper@mikroelektronik.fraunhofer.de

Abstract

During the start-up of the APECS Pilot Line, four application areas of advanced heterogeneous integration are addressed by the realization of demonstrators that highlight and evaluate the combined capabilities of the pan-European project partners. In this paper all four challenges in microelectronics will be addressed in detail:

High Performance Computing (HPC): HPC is driven by bandwidth requirements to enable increasing computing performance. Two general approaches are suitable to meet these requirements: Increasing the frequency and using finer pitches to widen the interface. A combination of both is not excluded. Heterogenous integration is required to combine chiplets and high-end packaging technologies, like fine-pitch silicon interposers. For the HPC demonstrator System-Technology-Co-Design (STCO) concepts will be enabled to co-design and co-optimize the system along all components and the used range of integration technologies. Based on the requirements this will lead to a first-time right functionality from the design to manufacturing and followed by verification measurements to confirm simulations.

Sensor-Integration: This demonstrator addresses the packaging and integration of multi-material sensor components, ranging from CMOS via Post-CMOS and C to III-V. Besides their material aspects, the sensor interfaces are to be adjusted in co-design with their heterogeneous system interposers and sensor frontends (digital and mixed signal) to enable cost-efficient chiplet integration for rapid development of sensor components in application relevant integration levels. The range of envisaged sensor components covers acoustic, optically active (light steering as well as detection) as well as gas- and magnetic-sensing chiplets.

Photonic-Integration: For this demonstrator an InP EML array chiplet will be integrated with an InP-HBT EML driver chiplet on a common interposer and coupled to an optical fiber array. The electrical high-speed connection between EML 4-array and driver uses polymer-based RF flexlines. Therefore, the photonic integration pilot line capabilities will be proved with a hybrid integration of InP chiplets on an interposer with photonic wire bonds (PWB) for the optical fiber coupling to a glass-based connector. A hybrid integrated high shoreline density o-band 4 channel transmitter (4x200Gb/s) for I/O in HPC systems will be realized.

RF-integration: For RF-integration three types of independent demonstrators will be developed: The first demonstrator will integrate InP chiplets on SiGe-BiCMOS as a D-Band transceiver. Secondly, by integration of mHEMT and SiGe-BiCMOS chiplets on Si-based interposer an H-Band transceiver for 6G will be demonstrated. Finally, a D-Band Radar and sensing module will be developed as two sub-parts of a third demonstrator. The last module consists of a Fan-out Wafer Level Package combining D-Band communication chiplets with radar TX/RX transceiver on RF-Glass Interposer with integrated antenna. Both parts will be connected by a flex-polymer bridge.

1 Introduction

The chosen APECS demonstration scenarios validate the pilot line operation by utilization of the conceived decentralized design and process capabilities. In particular the logistical and technological interfaces between different cleanrooms of varying wafer diameters (e.g. 2”-12”) and contamination requirements. The aim is not only to optimize the transfer between processing steps, but also to enable process combinations that expand the capabilities of chiplet technologies and hetero integration alike while maintaining efficiency close to a centralized process environment.

The resulting demonstrators were chosen to address most current challenges in microelectronics and yield chiplets ready for integration or chiplet modules.

2 High Performance Computing

The HPC demonstrator of the APECS project shows how high bandwidth data transfer requirements of high-performance computing can be tackled according to different needs for different applications. The example of a typical scalable RISC-V compute platform (Figure 1) is complemented by an AI at the edge example (Figure 2) that show both “high performance” but have completely different implications (Table 1) and therefore different chiplet module solutions at the end of the System-Technology-Co-Optimization, which is needed for designing each system.

As an example, this starts with the interfaces to supply data from the outside where the first uses PCIe for a compatible link to other computing platforms and the second uses a 2.4 GHz low power communication link. We show here that some crucial points are the partitioning and the design of the interfaces, but there are many more objectives coming from the market, the supply chain, the application etc..

2.1 Common reasons, why compute systems should be split into chiplets

For the scalability of both systems, it is very advantageous to have separate chiplets for peripheral communication and for computing. In both cases computing power scales with the number of computing chiplets while for most use cases a single peripheral chiplet will suffice. Also, the demands on interfacing change in a different time scale as the demands on computing so there might be more different compute chiplets than peripheral chiplets over time. Furthermore, the decision to have memory inside or beside the compute chiplets shapes the systems in terms of power consumption and ability, not only to be able to compute on streams, but also on larger chunks of data at a time.

2.2 Focus on electrical interfaces and objectives of the System-Technology-Co-Optimization

Since the market seems to focus on UCIe for the expansion and interconnection of compute chiplets in industrial and automotive applications this interface is used in the first case to interconnect peripheral and compute chiplets.

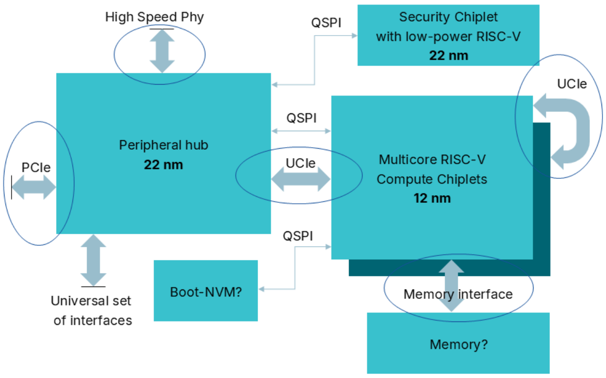

Figure 1 Industrial high-performance compute-system split into chiplets and the electrical interfaces in focus of the STCO

For the memory interface the choice is not so clear. There are several options of TRL in the market between DDR4, which is reliable, but already announced to be phased off by some memory vendors and High Bandwidth Memory, which has such a high density of wiring that the interconnect technology is very costly and still under development. Thus, the availability for a certain period and the cost of memory chiplets in the market have a heavy impact on the outcome of the STCO process, always in focus on the targeted products.

Since the RISC-V compute chiplets will use tens of watts of power there is enough energy available for the UCIe interfaces intended to operate most of the time.

For the edge AI computing example shown in Figure 2, where the neural computing units consume only hundreds of mW and where the expansion and memory interfaces are more likely to work only part time, there is the need for different solutions for these interfaces. Table 1 illustrates a few of the differences in STCO objectives for both systems.

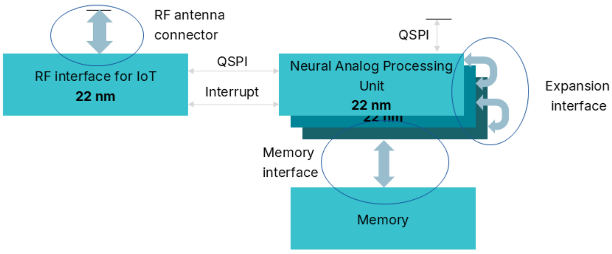

Figure 2 High performance compute-system for AI at the edge and the electrical interfaces in focus of the STCO.

STCO objective	**RISC-V compute chiplet module**	**AI at the edge compute chiplet module**
Definition of „high performance“	Compute operations per second: TOPS (speed)	Compute operations per watt: TOPS/W (efficiency)
Highest BW signal	UCIe data lines, 8 GB/s SerDes	2.4 GHz RF
“on” to “off” ratio	Always on	Always on and sparsely on
„off“ leakage power	mW	10uW… 100 nW

Table 1 Different STCO objectives for two HPC systems

These are only a few aspects to show how the STCO process is fed by constraints to find an adequate solution.

2.3 Possible solutions for building an HPC chiplet system

Depending on the outcomes of the STCO there are different opportunities in the APECS production line to create a chiplet module like it is sketched in Figure 3. The wafer-level interposer might be realized e.g. as silicon interposer or as a RDL$^{\text{1st}}$ based technology. Since the advanced organic package substrate RDL fineline wiring capabilities merge versus wafer-level based interposer technologies, there might even the chance to go without an interposer for the AI case. Wafer-level interposer technology can be varied between Si interposer with inorganic RDL incl. TSV or RDL$^{\text{1st}}$ based organic RDL approaches depending on I/O density.

Chiplets might be placed on interposer or on the package substrate depending on the interface connection density. Mainly for medium-bandwidth memory this is an option.

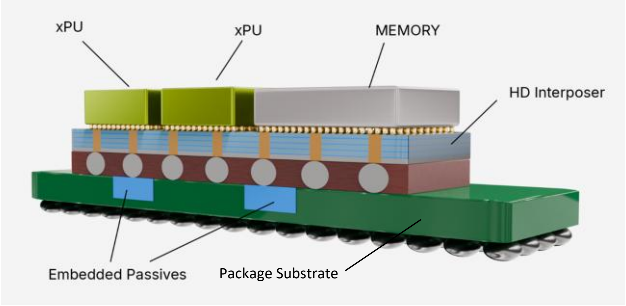

Figure 3 Exemplary chiplet module of the HPC demonstrator.

3 Multi-Material Sensor

Semiconductor sensor systems are becoming increasingly complex and highly specialized based on the sensing modality. As such each type of sensor has unique integration and packaging challenges. Additionally, for most modern sensors an increasingly level of in sensor data processing is desired to increase the overall system efficiency, reduce communication bandwidths and partition system components. These challenges are addressed in the Multi-Material Sensor (MMS) demonstrator (see Figure 4) that pushes current heterogeneous processing and integration capabilities by combining MMS-chiplets with heterogeneous system interposers and advanced sensor frontends (digital and mixed-signal). The latter can be augmented with additive neuromorphic accelerators for utmost energy efficiency and latency.

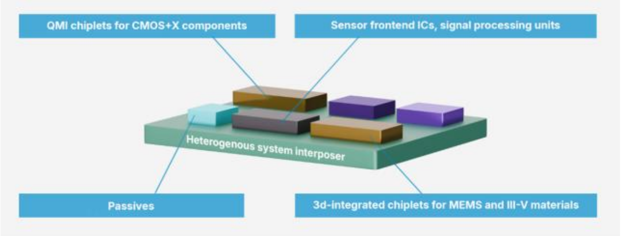

Figure 4 Generic multi-material sensor system schematic and its building blocks.

Based on an initial sensor chiplet technology selection among the APECS partners, a diverse set of application domains with their unique technological emphases has been chosen to be addressed in this demonstrator – namely optical, gas, magnetic field and acoustic sensing.

Following the distributed pilot line approach and a common STCO approach among all application areas, discrete processing and integration value chains are realized within APECS. The resulting IP portfolio shall offer design flexibility and fast development times for different applications. The processing steps are selected to be scalable for pilot series production. As such, the different combinations of components compose a versatile and generic approach towards end-to-end design flows and methodologies for chiplet-based advanced heterogeneous system integration.

3.1 Sensing Chiplet Peculiarities

In this context the optical sensing activities a piezoelectric MEMS mirror for beam steering and illumination control as well as QMI-integrated PICs on CMOS technologies for light detection and interferometry are being utilized. Both sensor technologies are to be developed into 3D-integratable sensing chiplets and require optical access limiting possible integration strategies. To achieve optimal performance of the moving MEMS component, it is embedded into a hermetic modular glass housing, i.e. glass dome and (thick) glass interposer with integrated getter functionalization as well as TGVs. For the PIC integration its scaling towards array compatibility with CMOS photodetectors or read out integrated circuits (ROIC) and subsequent thermal management during operation remains a challenge to be addressed.

The gas sensing components utilize emerging GaN-based sensing technologies which require high-thermal budget during processing and a not CMOS compatible functionalization to enhance its sensing performance. Additionally, gas penetration barriers can be employed to mitigate sensitivity towards undesired gases and shield reference sensor networks. For certain gases, e.g. corrosive gases, the chiplet technology requires specific passivation and metallization to improve its lifetime.

In case of the magnetic field sensing, both QMI integrated CMOS and III-V technologies are employed. During their chiplet integration, emphasis is required on thoughtful power routing to mitigate or compensate magnetic fields within the sensing chiplet itself.

Similarly, for the acoustic sensing domain CMOS-compatible MEMS technologies (i.e. CMUT arrays) are being QMI-integrated with CMOS components while improving their signal quality and maintaining the mechanical connection to the interposer.

3.2 (Co-)Integration challenges

Due to the diversity of the envisaged combination of sensor technologies, their processing in a singular process environment or even monolithically is not possible due to contamination restrictions and incompatible thermal budgets during processing. Hence, they are commonly partitioned into sensing chiplets. At this point challenges are transferred to their (co-)integration where typically specialized solutions are developed to match individual integration and signal processing challenges. In contrast, the MMS-demonstrator aims to create a building block-based integration approach to address a multitude of sensor systems by yielding chiplet modules with integrated sensor frontends. This way, not only the material but also electrical and signal domains are partitioned, and the complexity of following integration steps is significantly reduced. Besides mechanical challenges, this requires strategies on handling different supply voltages (up to ~100V) and currents (up to ~1A per pin) towards different chiplets. At the same time signal integrity should not suffer in comparison to specialized solutions. Since no common interface standards are employed, especially for emerging chiplet technologies, the chiplet interface requires a certain degree of flexibility. To achieve this emphasis is placed in the development of a heterogeneous system interposer, which is to be compatible in its utilization with all above-mentioned sensing chiplet technologies. In addition to the sensing chiplet and interposer, a flexible sensor frontend and a chiplet-based neuromorphic accelerator are utilized.

3.3 Design for MMS-Chiplet Modules

The combination of diverse sensor components spans different multi-physics domains, design tools and maturities of A/PDKs used for their development. To ease these challenges, it is envisaged to partitioning the design and optimization flows yielding well defined design interfaces and parametrized behavioral models of other system components, allowing for distributed component development.

4 Photonics Integration

New technological advancements, such as the Internet of Things (IoT), Big Data, and Artificial Intelligence (AI), cloud computing, and data centers, resulted in a strongly increased demand for high-speed, low-latency, and scalable solutions for data transmission. Therefore, there is a huge need to develop cost-effective, energy-efficient, and compact optical 200G (or even higher) optical interconnects. However, at 200G and beyond conventional electrical bonding techniques come to its limit because of high electrical loss. So, hybrid photonic integration of transmitter/receiver chiplets and the corresponding driver chiplets is an essential requirement allowing for short high speed electrical connections between them.

4.1 Photonic chips

Within APECS technologies to realize such photonic chiplets will be advanced and developed. A schematic cross-sectional view of such a photonic sub-assembly is shown in Figure 5:

A III-V based driver chiplet is hybridly integrated with a III-V based transmitter chips allowing for short and low loss electrical connections. The underlying distribution layer serves for the distribution of the electrical signals and transmits the generated heat. The interposer will also carry the electrical connector at the input side and the optical fiber connection at the output side.

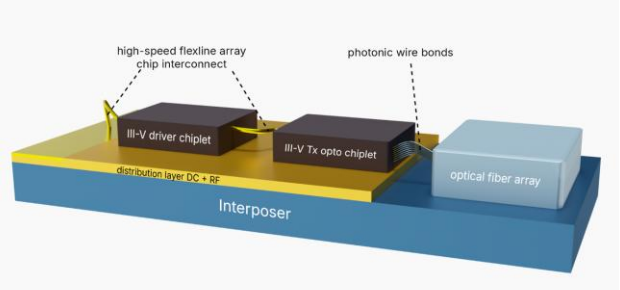

Figure 5 Schematic view of a hybridly integrated high speed photonic transmitter sub-assembly.

4.2 Photonic transmitter chip

As a concrete example for such a photonic chip within APECS an O-Band 4 x 200 G transmitter with high shore line density for I/O in HPC will be realized comprising a narrow-pitch InP-based 4 x 200 G EML array chip and corresponding InP based driver chip hybridly integrated on an interposer. This interposer serves for an efficient heat dissipation, carries the electrical feeding lines (RDL) and the electrical connectors. The fiber coupling of the EML array chip will be realized using photonic wire bonds (PWB).

Such high-performance photonic chips require not only benchmark optical and electrical chips but also ultra-low loss optical and electrical interfaces between these components plus efficient heat dissipation. Within APECS all these aspects will be considered, covered and addressed in order to achieve a full functional 4x200G photonic transmitter sub-assembly.

The developed technologies within APECS will then allow to realize a large variety of complex hybridly integrated high speed photonic subassemblies in future, so that these capabilities then can be offered to external customers.

4.3 Photonic Wire Bonding

The interposer has to be structured by advanced etching techniques to allow short 3D electrical interconnects by high-speed-flexline arrays (see left in Figure 5 & 6). The PWBs will interconnect the 4 EML waveguides with 4 optical fibers for interconnecting the output signals to the system (Figure 6).

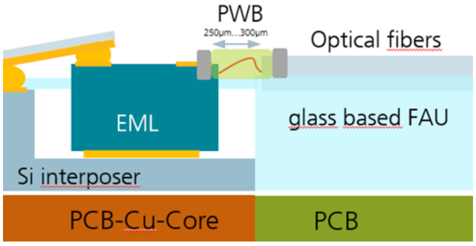

Figure 6 Schematic drawing of the optical interconnect to be realized by innovative two photon polymerization (TPP). The FAU (light blueish).

The innovative FAU will be made by selective laser induced etching (SLE) and features V-grooves and mechanical alignment supports for z-dimension to the Si-interposer. In Figure 7 the pitch converter platform for TPP parameter setting and performance optimization is shown.

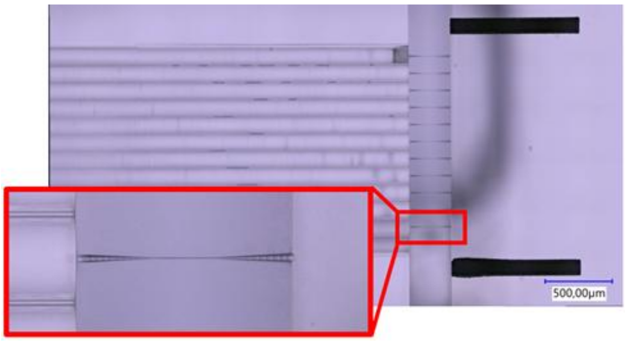

Figure 7 Test sample to interconnect optically an12- channel optical fiber array unit (FAU, see left side of the micrograph) to an 12 channel integrated optical waveguide array (right in between the two black alignment marks) by PWB using TPP (see one of them enlarged within the inset)

The fiber mode fields are matched to the integrated waveguides within the pitch converter platform at 1550 nm optical wavelength.

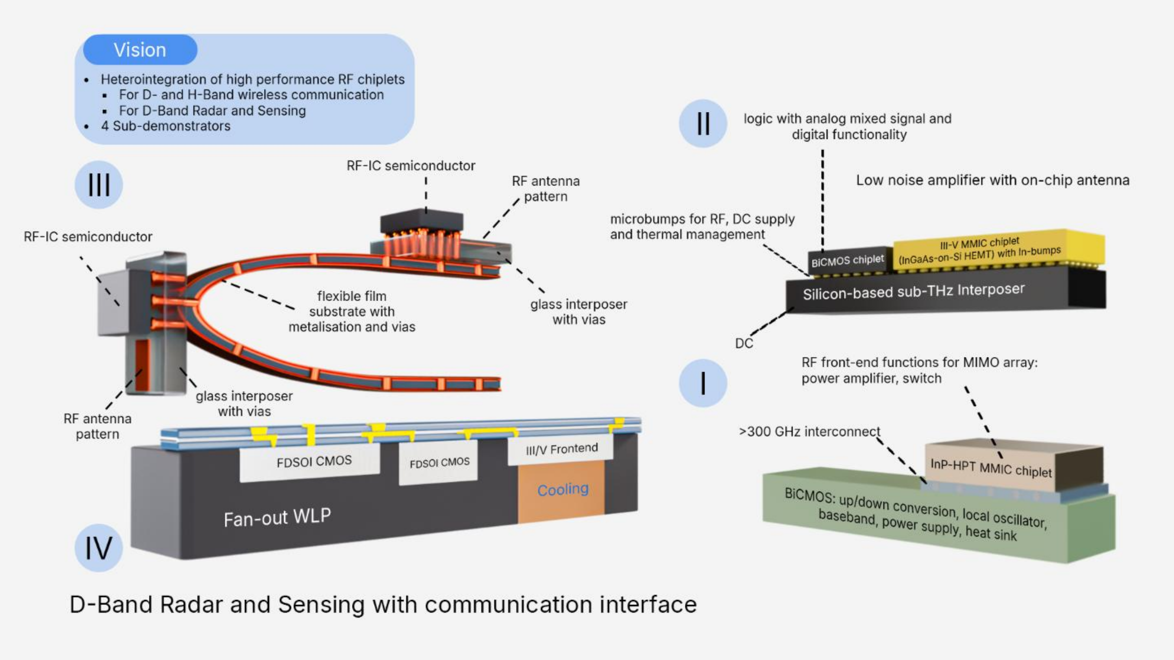

Figure 8 Overview of the RF-related demonstrators within the APECS pilot line

5 RF Integration

In the APECS pilot line, due to four advanced demonstrators in the Radio Frequency (RF) domain, the heterogenous integration capabilities for integrated RF systems up to 300 GHz will be demonstrated. The goal of the APECS pilot line in the RF domain lies in the enablement of complex chiplet modules, which combines the most beneficial semiconductor technologies for the different system parts within the RF domain. This means for example III/V semiconductor technologies for the first and last stage of a transceiver with high performance BiCMOS Technologies for the more complex RF system parts in the transceiver. The relevant RF chip technologies, which are targeting with the four demonstrators are:

- (Bi)CMOS: SiGe-BiCMOS,
- FDSOI-CMOS,
- GaN-on-SiC HEMT,
- InP HBT,
- InGaAs mHEMT.

5.1 Overview of the RF demonstrators

In Figure 8, the four RF-related demonstrators (I to IV) are shown. Besides a subdivision into different use application scenarios in the field of wireless communication and radar-based sensing, a subdivision can also be made into different kinds of integration technologies.

5.2 RF-compatible integration technologies

In the APECS pilot line, two general paths for integrating high performance systems in the Radio Wireless domain up to the Sub-THz regime will be setup and be ready for use. In particular, it is a quasi-monolithic integration (introduces by Intel), presented in 5.2.1 and 2.5/3D heterogenous integration, which is highlighted in 5.2.2.

5.2.1 Quasi-Monolithic Integration (QMI)

The advantage of a quasi-monolithic integration technology, which is part of the APECS pilot line, lies in the possibility of creating compact modules, which can easily integrate into complex systems by using well known assembly technologies. From a high-frequency technology perspective, it enables wafer-based modules, which contains all high-frequency parts and signal routing within this module and offers easier routing of low-frequency signals to the system interfaces.

5.2.2 2.5/3D heterogenous integration

The 2.5/3D heterogenous integration covers and combines a very broad range of technologies. In APECS, especially the functional interposers, stacked wafer technologies and functional integration to chiplets and advanced packaging and assembly technologies will be combined. The resulting capabilities will be shown by means of RF demonstrators.

5.3 Detailed analysis of the demonstrators

In 5.3.1, two demonstrators will be proposed to show the capabilities of the APECS pilot line in terms of QMI integration for wireless millimeter wave 6G communication frontends. In 5.3.2, a demonstrator, which represent a radar-based sensing frontend and an associated wireless communication interface will be shown, to demonstrate the major capabilities of the APECS pilot line for this kind of systems.

5.3.1 QMI integration for 6G communication

The implementation of the QMI integration technology in the APECS pilot line enables the combination of system parts, which are realized in BiCMOS and III/V semiconductor technologies. This will be demonstrated by demonstrator I and II, which are shown in Figure 8. In particular, in case of demonstrator I the combination of BiCMOS with InP HBT technology will be realized and in demonstrator II BiCMOS with InGaAs-on-Si HEMT will be realized as a stacked solution, as shown in Figure 8. The later one will allow 6G frontends up to 300 GHz. With the extension in output power, which comes possible due the use of InGaAs-on-Si HEMT, this approach will overcome the performance of pure BiCMOS frontends at frequencies up to 300 GHz. In demonstrator II, the combination of BiCMOS for the complex system parts of the whole frontend, which claim higher integration density, and InGaAs-on-Si HEMT will be realized. Key innovations here will be a new low inductance via technology and an additional metal layer for interconnects to the existing metal layers. Both key innovations will enable significantly more complex RF systems, which are highly necessary for 6G communication interfaces.

Based on the QMI technology, which is part of the APECS pilot line, two integration setups will be presented: In case of demonstrator I (Figure 8), the QMI technology will be used to realize a stack of BiCMOS and InP HBT technology, which represent a vertical integration. With demonstrator II, a horizontal connection, realized in different semiconductor technologies, will be shown. Here, a silicon-based interposer acts as a carrier and base for the interconnects in millimeter and sub-THz range.

5.3.2 2.5/3D integration for radar-based sensing

For the demonstration of the 2.5/3D heterogenous integration capabilities, two demonstrators will be realized, which are associated to each other. The first demonstrator for radar-based sensing, (Figure 8, III), comprise a radar front end in BiCMOS technology. The key innovation here is that radar front ends in the D-Band regime are mounted onto RF-Glass Interposer. The RF-Glass Interposer is also the carrier substrate to realize a planar antenna array. This enables compact, high performance radar modules, which contain all millimeter wave signalling. To allow the integration onto non-planar and also bending surfaces, these radar modules are mounted onto a flex polymer substrate carrier, as shown in Figure 8 part III. With this approach, a distributed Multi-Module Radar can be realized on non-planar and/or bending surfaces, like drones, wind turbine wings, airplanes, etc.. To enable for such use cases also a wireless, high-data rate interface an adapted communication interface will be realized as a separate but associated demonstrator IV (Figure 8). Here, a multi-channel communication transceiver frontend is combined with a PA and an LNA module to improve the output power and noise performance of the communication transceiver. Furthermore, an analog-to-digital converter (ADC) will be implemented. Both demonstrators combine different semiconductor and 2.5/3D heterogenous integration technologies. In the case of demonstrator III, the focus lies on the combination of a RF-Glass interposer and flex polymer technology. Both technologies offer the advantage, that very precise and fine spaced structures are possible, because of the use of a lithography. This enables radar-based sensing modules in the millimetre wave and sub-THz regime, because a state-of-the-art BiCMOS semiconductor technology can be integrated in this module and it can be ensured that the full RF performance of this semiconductor technology can be used, because of very less losses. In demonstrator IV, the focus lies on the combination of different chiplets to a communication interface module. The package technology used here is a fan-out wafer level package (WLP). In this package, a 22nm FDSOI CMOS ADC and multi-channel frontend will be implemented, as well as a III/V-based PA/LNA stage for performance and therefore range extension. The challenge here is the power management and the integration of cooling structures into the package.

6 Conclusion

The demonstrators in APECS will show the seamless cooperation of 15 institutes within the pilot line. Nearly all hetero integration technologies will be implemented in a final set of seven independent modules. These will address core tasks in microelectronics, such as high-performance computing, modular sensor technology, data and telecommunications, and radar technology. Beyond the technological approaches, the principle of system technology co-optimization (STCO) will help to respond quickly and in a resource-efficient manner to the requirements of industry.

7 Acknowledgement

The work presented was carried out in the framework of the APECS Pilot Line of the Chips Joint Undertaking, funded by Horizon Europe (ID: 101183307) and Digital Europe (ID: 101182906) Programs and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain.

8 Disclaimer