Vision of the APECS Pilot Line

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Abstract

Heterogeneous Integration for Electronic Components and Systems and Advanced Packaging (APECS) is essential for the sovereignty and competitive advantage in areas such as telecommunications, high-performance computing (HPC), Artificial Intelligence/Machine Learning (AI/ML), sensor systems, medical & scientific instrumentation and industrial manufacturing in Europe. The goal of the APECS Pilot Line (APECS-PL) is to enable European users to benefit from chiplets of various technologies, from any supplier (European or international). The APECS pilot line will therefore offer necessary services, capabilities and training for European companies, especially SMEs, to integrate and package chiplets into novel electronic components and systems. The platform of capabilities to be developed will include novel characterization, quality assurance, testing & reliability (CTR) methodologies and a System-Technology Co-Design (STCO) framework to ensure quality, reliability and fast production ramp-up in collaborating manufacturing organizations. In this paper the motivation and the vision will be explained in details as future microelectronic systems will require higher levels of functionality that cannot be managed by a single chip, even if advanced System-on-Chip (SoC) concepts are applied. Instead of manufacturing one large semiconductor chip and then packaging it as single monolithic IC component, the IC is broken down into various smaller parts, chiplets. The assembly of these multiple small chiplets into a complex, and often three-dimensional package leads to highly integrated system components. Using a modular design, many individual solutions can be implemented by interconnecting different basic functionalities. Special functions, such as RF, optical, sensing or other structures can be manufactured using optimal technologies on external wafers and in different structure sizes. The chiplets in the APCES-PL will be connected on special substrates (e.g. Si, glass, or organic) side-side-by-side (called 2,5D) or stacked (called 3D). The APECS-PL will provide open access in accordance with the Chips Act requirements by providing support to integrated production facilities and open EU foundries, SMEs and startups, through preferential access to the new pilot line, as well as by ensuring access on fair terms for a wide range of users of the Union's semiconductor ecosystem.

1 Introduction

Europe hosts a dynamic network of tech champions, spanning traditional IDMs, foundries, material and equipment suppliers, and design/test houses, all the way to integrators, OEMs, and vertical industries. It also includes SMEs, startups, and research and technology organizations (RTOs). EU economic needs favor high-value capital goods produced in smaller to mid-sized runs rather than mass-market consumer products. Yet European firms often struggle to scale due to restricted access to advanced semiconductors and integration technologies.

The EU Chips Act is therefore an important step toward strengthening Europe's microelectronics industry. It aims to close the gap between cutting-edge research, innovation capability, and sustainable industrial use—a crucial factor in an increasingly digital world that relies more and more on microelectronics production. Through targeted funding under the EU Chips Act, the EU will be able to boost its own competitiveness and assume a leading role in the global semiconductor market. The goals pursued by the Chips Act are to be achieved through three strategic pillars.

2 Structure of the APECS-PL

The APECS pilot line is part of the "Chips for Europe Initiative," which aims to support the large-scale development of technological capabilities and innovations across the entire EU and to advance the development and deployment of advanced semiconductor and related technologies, such as quantum technologies. "APECS," short for Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems, brings together the competencies, infrastructures, and know-how of ten partners from eight European countries. In Germany, twelve institutes of the Fraunhofer Society (project coordinator) and two institutes of the Leibniz Association are involved in the pilot line. APECS is implemented by the FMD—the globally leading, cross-site R&D consortium for micro- and nanoelectronics. APECS is intended to become a long-term accessible pilot line for all European stakeholders across the entire value chain. Together with the other pilot lines implemented under the EU Chips Act, APECS is a key component for heterogeneous integration and advanced packaging within an overarching, pan-European microelectronics pilot line. To achieve this goal, existing collaborations with European partners will be expanded and strengthened.

3 Mission of the APECS-PL

In line with the EU Chips Act, APECS aims to help close the gap between research, industry, and policy to boost Europe's international competitiveness in advanced packaging and heterogeneous integration. Furthermore, the pilot

line will be a driving force in advancing the next generation of integrated microelectronic systems. By bringing together diverse technologies, advancing European collaborations, and providing seamless access to innovative solutions, APECS seeks to build a community of interest that enables research institutions and companies—from startups to SMEs to industry leaders—to play a key role in the global microelectronics market. All developments will be conducted in line with the requirements of *the European Green Deal*.

4 Expected Impacts

The APECS pilot line enables European companies, especially startups and SMEs, to access essential services, expertise, and training to integrate chiplets into novel electronic components and systems. It opens up entirely new markets and opportunities for European business models in the following areas and application areas:
• advanced technologies for custom applications
• groundbreaking process integration concepts
• short time-to-market
• strong ecosystem
• smooth knowledge transfer
• latest measurement and testing techniques for characterization and fault analysis
• testing from component level to system
• holistic system reliability considerations
• complete system design (P/ADK design flows)

Application areas:
• Telecommunications
• Artificial Intelligence / Machine Learning (AI/ML)
• Medical devices
• High-Performance Computing (HPC)
• Sensor systems
• Industrial manufacturing

5 Implementation and Access

In the strong European consortium, APECS combines the technological competencies, infrastructures, and know-how of ten partners from eight European countries: Germany (Fraunhofer Society, Leibniz–Association), Austria (TU Graz), Finland (VTT), Belgium (imec), France (CEA-Leti), Greece (FORTH), Spain (IMB-CNM, CSIC), and Portugal (INL). The APECS pilot line is coordinated by Fraunhofer-Gesellschaft and implemented by the Research Factory Microelectronics Germany (FMD).

The APECS Pilot Line targets the entire European microelectronics industry, from startups and SMEs to large companies, including automotive suppliers and research institutions. Access is open to everyone. APECS offers therefore a self-contained platform for all participants in the value chain, from foundries and Integrated Device Manufacturers (IDMs) to Outsourced Semiconductor Assembly and Test (OSAT) and to microsystems technology and electronics users, training organizations, universities, test houses, and material suppliers. The APECS Pilot Line focuses on collaboration with European institutions. Since microelectronics development is cross-border, is it also planned to install collaborations with Japan, Taiwan, South Korea, the United States and other countries.

The APECS Pilot Line builds a bridge between research and industrial implementation. The partners on the pilot lines jointly develop technologies that are often too complex, time-consuming, or costly for individual companies. The goal is to enable partners to test, implement, and transfer modern technologies to their production with minimal barriers for new concepts. This gives companies clear guidance on which equipment they need for specific processes and which conditions are decisive for making the optimal choice for their product portfolios.

APECS supports industrial uptake through:
• Design Services – Enabling chip, chiplet IP, and system design with expert-supported platforms
• Process Development and Validation – Accelerating the commercialization of new materials, tools, and processes
• System Development – Facilitating the creation of advanced AI, automotive, and industrial applications
• Manufacturing Outsourcing – Providing proof-of-concept, prototyping, small-volume production, and scalable transfer pathways
• Research Access – Streamlining the transition from research to application through local competence centers
Details of these topics will be presented in the other papers and talks of the session.

Instead of saying something is technically impossible or too complex, the APECS Pilot Line should help implement new ideas and open up new markets. Research institutes, startups, and SMEs should have easy access to produce hardware prototypes in small series of several hundred units for new ideas. At Fraunhofer IZM, the Start-a-Factory is already showing how this works successfully. With APECS, the approach will be extended in the field of high-technology. This is not only about silicon chips, but also about RF chips based on III-V semiconductors, as well as MEMS and optoelectronic components. The entire concept should be extended to additional manufacturing technologies in semiconductor technology.

The research infrastructure will be distributed across multiple Fraunhofer locations. A Manufacturing Execution System (MES) will ensure the complete run-through and transport of chips and wafers between the participating facilities. A major advantage is the ability to work with different materials, since not all can be processed in a cleanroom, e.g., gold. Furthermore, every Fraunhofer Institute and every Leibniz Institute is closely linked to one or more university facilities, which contributes an additional significant scientific impulse to the research by bringing in local excellence competencies. The use cases for chiplets are very diverse: wherever extremely high computing power

and very high integration density are required, e.g., for AI applications in automotive and industrial electronics. In addition to High Performance Computing (HPC) and AI clusters, scenarios are conceivable where data processing occurs directly at the sensor node (Edge AI) with the help of artificial intelligence—i.e., at the point of data collection. It is conceivable that in industrial electronics, complex image processing occurs directly at the sensor node. Highly integrated chiplets in an optimized combination of computing, power delivery, and wireless technologies could become a "game changer." The entry point for collaboration with the APECS Pilot Line can be diverse. The APECS Pilot Line fundamentally supports the development of a holistic system design and conveys process understanding. This includes defining chiplet interfaces, substrate fabrication, reliability testing, and manufacturing a complete chiplet module.

To prototype and mature the pilot line during the implementation phase and the expansion of existing FMD lines, four demonstrators are planned. They will illustrate how the building blocks of the pilot line work together and how the developed processes can be combined. These capabilities are to be further expanded in collaboration with the other project partners and collaborating external research organizations (RTOs). Details of the demonstrators will be explained in a separate paper of the session.

Typically, companies already have an approach to implementing a chiplet module but need support developing an organic interposer for example. In that case, the entry point would be a project to realize an organic interposer for chiplets and to produce a functional chiplet module. Companies could also receive training on advanced processes, request contract research, or conduct exclusive pilot productions of small series. The APECS Pilot Line offers tailored access models and solutions to European partners for such scenarios.

The FMD Office operates in a versatile manner: it handles full project management and marketing, coordinates equipment procurement, and leads the development of demonstrations. It also serves as the central interface to project sponsors at the German and European levels and acts as a matchmaker for European semiconductor technology. To demonstrate the functionality of the APECS Pilot Line, four demonstrators will be developed, covering different areas of the technological portfolio: radio-frequency technology, optoelectronics, high-performance computing, and MEMS integration. There is no formal process or pre-made solutions; the key is conversation. In discussions with subject matter experts, it often becomes clearer for customers what they really need and which additional aspects, such as chip design, must be considered. With the APECS consulting services, tailored solution approaches are offered.

6 Summary: Project Goals

• Meet the microelectronic core needs of European industry and research
• Establish national know-how at the European level
• Drive European collaboration across all levels of the microelectronics value chain
• Promote European competitiveness at the highest level
• Further the development of heterogeneous integration through the latest packaging technologies
• Create new perspectives for regional system and chip manufacturing

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