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APECS Pilot Line: Your Gateway to Heterogeneous Integration & Packaging Technologies

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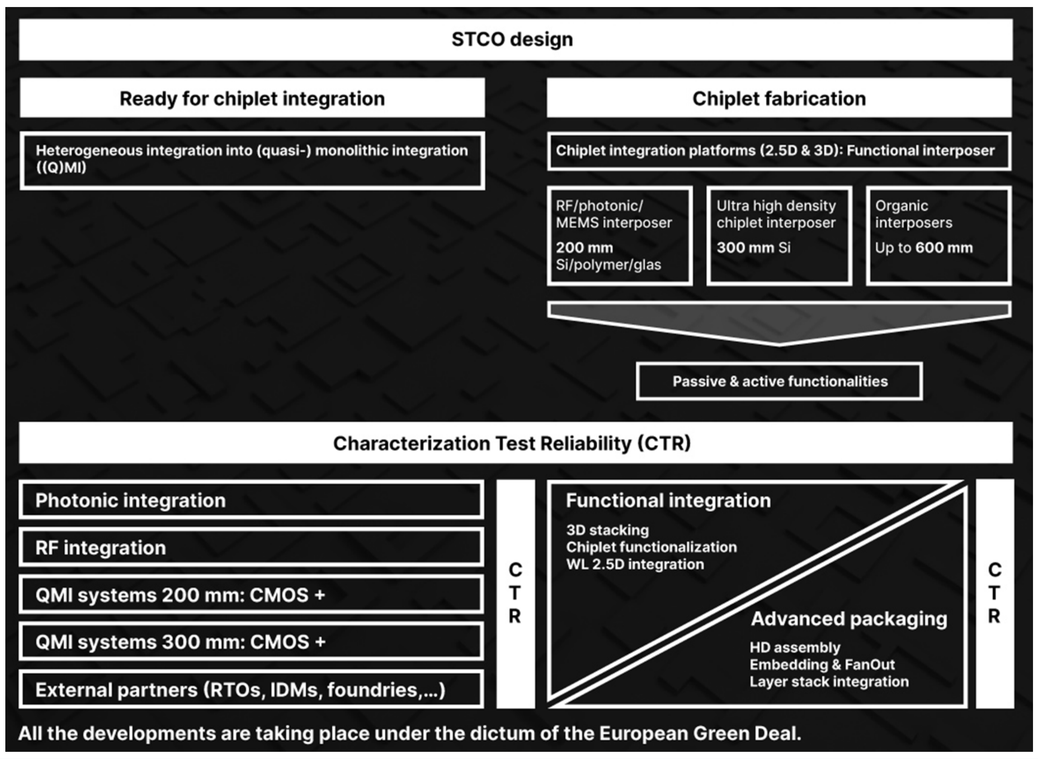
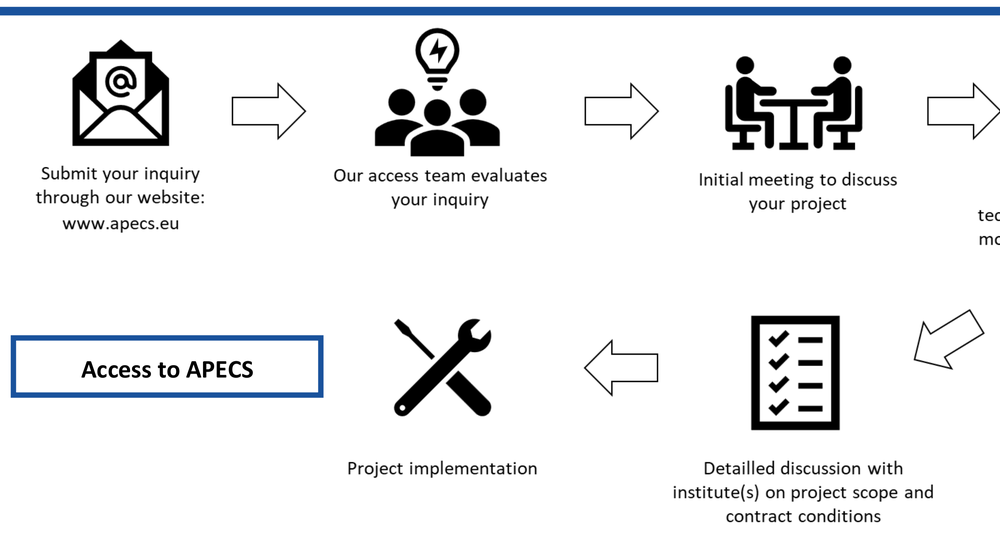
The APECS Pilot Line

- Is an open-access technology platform covering the full semiconductor value chain in Europe
- Provides services from chiplet design & development to packaging, characterization, testing and reliability assesment
- Offers State-of-the-art and advanced equipment for scalable proto-typing
- Accelerates innovation and technology transfer
- Enables efficient and reliable market entry for current and next-generation microelectronics
- **APECS aims to build a strong foundation for a resilient and robust European semiconductor supply chain**



Challenges in Heterogeneous Integration

- Design complexity
  - Integration of diverse materials, functions, and system domains
- Manufacturing precision and testability
  - High precision, yield optimization by in-line testing, and process control
- Reliability, standardization & interoperability
  - Definition of universal design rules, standardizing interfaces, and reliability benchmarks
- Cost management
  - High manufacturing costs and need for efficient, scalable production



What APECS offers

APECS offers the services, capabilities and training needed by European companies and academia, to design, integrate and package any kinds of chips/chiplets into novel electronic devices and systems. The APECS technology portfolio consists of four objectives:

- Diverse heterogeneous integration & advanced packaging solutions of chips/chiplets
- Testing, reliability & security of devices and systems
- Process customization for chiplet manufacturing and integration
- Prototyping & viable scalable production from pilot to industrial level

Annual Open Calls

- Opening: April 1st 2026
- Closing: June 30th 2026 at 23h59 CET (deadline for submissions)

Technologies covered in Open Call

- CTR (charaterization, test and reliabilty) services
- Integration and Packaging Technologies
- MPW Runs
- Imaging Technologies, Post-CMOS Photonic Platform and IPD (integrated passive devices) planar components

Who benefits and how

- Chip Foundries & IDMs
- Materials and tools suppliers & semiconductor customers
- Start-ups and SMEs
- Research & academia

Benefit from

- Design services and prototyping
- Process development & validation
- System development, manufacturing outsourcing
- Access to research & infrastructure

Contact

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Additional information

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