Advanced Heterogeneous System Integration of Chiplets and Quasi-Monolithic Integration

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Abstract

The increasingly higher costs for further node miniaturization in the IC manufacturing process will promote the interconnection of chiplets. The increasing miniaturization of semiconductor structures and the associated increase in technology complexity have led to an enormous increase in the cost of IC production. The idea now is to use different types of IPs that can be used for specific functions. Starting with solutions in the microprocessor sector, chiplet integration technology also offers new opportunities for innovation in the areas of MEMS, RF and optical systems. However, advanced heterogeneous integration is therefore essential for the integration of such chiplets, which goes far beyond the known integration methods for monolithic processes, such as full-chip integration and 2.5D integration. These concepts must be further developed in line with the qualitative and quantitative changes in industry requirements. Special attention is also paid to the expansion of heterogeneous integration to quasi-monolithic integration (QMI) for maximum power density by utilizing back-end-of-line and advanced packaging capabilities. Novel back-end-of-line interface technologies for MEMS, opto/RF chips (III/V RF chips with (Bi)CMOS for frequencies above 100 GHz) to make "hard IP" (IP blocks, not only mapped in a library as in SoC, but actually in-silicon processed for further use) available are also planned, as well as world-leading test concepts and technologies for functionality, quality and yield optimization of heterogeneous integrated systems.

1 Introduction

With the EU Chips Act the European commission and the EU Parliament have set the stage for europe´s future role in the global microelectronics and semiconductor industry. As part of the pillar 1, which is set to reinforce the capabilities in the challenges for novel semiconductors and semiconductor based applications, in the first wave of activities five pilot lines were set on course to build capabilities and research capacities in the areas which will define the future of European electronics.

The APECS (Advanced Packaging for Electronic Components and Systems) is mostly located in the value chain right after the semiconductors have been processed, interfacing as early as the backend of line with the next steps in the value chain. Some technological chiplet aspects for components in the high-frequency and photonic range are also anchored in APECS. With the heterogeneous integration at hand, close collaborations with the two pilot lines dealing with advanced semiconductors, the pilot line Nano IC targeting 2nm advanced nodes and below, as well as 5nm FDSOI for next generation ultralow power systems (FAMES) is being established by hand-in-hand process chains. APECS will also focus on the new paradigm of chiplets, and their challenge to the traditional flow of building advanced SoC (System on Chip).

Here, as early as designing-in the chiplets with the standardized interfaces both on the signal as well the physical layer, through all steps of chiplet integration towards quality assurance and test, APECS is poised to cover all aspects of this paradigm extending from the digital world towards analog, RF, sensors and optical systems. Today the current status are complex heterogeneously integrated microelectronic components as the backbone of modern electronic state-of-the-art systems. There will be a significant increase in demand for heterogeneous integration in semiconductor technology in the future.

APECS has thus been set with building blocks (*Figure 1*), the one on "2.5 & 3D Chiplet Integration" being detailed here in the paper.

For chiplet and advanced IC integration, technology challenges are persistent through out each step of the process flow, building closely on top of each other to reach the functional system. Here, foremost, is bridging the gap from the huge number of interconnects required per mm^2

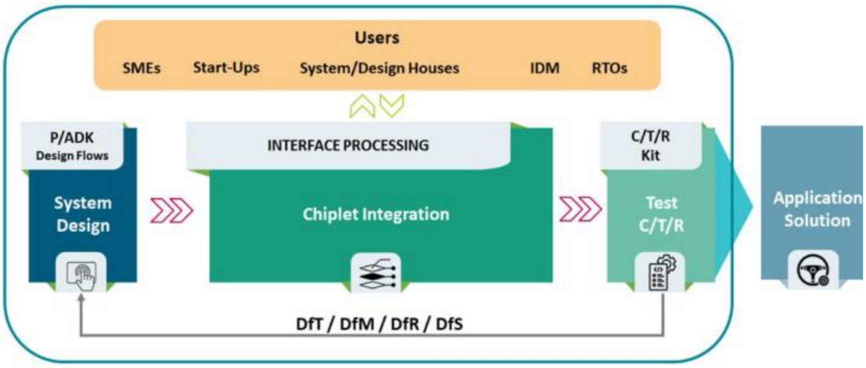

Figure 1: Structure of the APECS Pilot Line

for the advanced nodes to the next level of packaging (q.v. Figure 2).
To do this, advanced substrate technology is required, which can offer µm or even sub-µm interconnect pitches to match with the pads of the IC, resp. chiplet. Here, the last decade has seen a shrink of the necessary contact pitches from 100s to 10s of microns, now reaching down into the single digit micron scale and projected to target 200nm pad to pad spacing. With this breathtaking pace, traditional IC substrates based on laminate have been challenged to their limits. Silicon since has emerged as a solution, using advanced lithography and etching technique to realize Interposers (both passive and active) which provide highest density interconnects between neighboring chip(lets) and using Through Silicon Vias and re-routing on the backside of the interposer a match to state-of-the-art IC substrates.
APECS pushes the envelope here with its research on “Functional Interposers” using Si wafers with 300mm diameter up to novel panel scale alternatives based on organics or glass.
Assembling the ultrafine pitch chip(let)s to the interposer, securing their electrical and mechanical integrity during the subsequent process steps is the next challenge in the chain of process. Here, bonding processes to cater for the small pitches, large IC/chiplet dimensions and even stack-bonding in 3D are to be developed for manufacturing

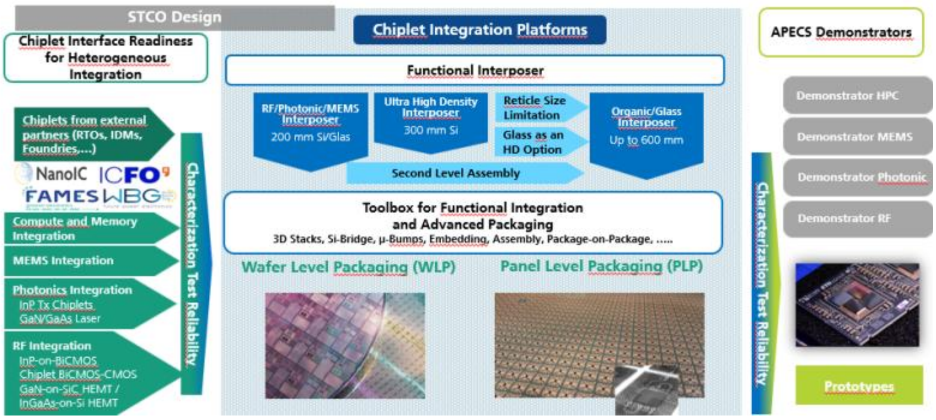

Figure 3: APECS pilot line modules, focus on QMI and 2.5/3D Integration

ready solutions. This research is conducted in the framework of the “Functional Integration” module of APECS.
Lastly, these highly functional sub-systems need to be merged with and to the final electrical systems, which will require advanced substrates and assembly techniques, offering SLP´s (substrate like PCB) compatible with the Si based sub-system and the next integration layer, which may be another PCB, a 3D shaped device carrier or even a panel scale system. The APECS module “Advanced Packaging and Assembly” addresses these challenges beyond the state of the art.

The specific challenges and solution approaches for the modules and their interface within each other and the supporting APECS elements (Design & Quality Assurance-CTR) to offer a Pilot Line encompassing all aspects from chiplet to system (Figure 2) will be described in the next section.

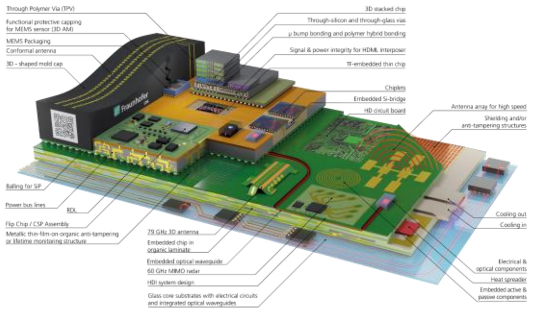
Figure 2: Electronic Packaging Levels from wafer to system (schematic)

2 APECS QMI and 2.5&3D Integration

2.1 Module “Quasi-Monolithic-Integration”

A specific and advanced kind of 2.5 integration is the Quasi-monolithic integration (QMI). QMI aims to use processes from standardized semiconductor and chip technology to produce different semiconductor components with a common back-end-of-line. The semiconductor components can be fully functional chiplets or partially processed chips known as dielets, which are only processed up to the contact level, for example. A key process for this approach is a wafer level, highly parallelized chiplet or dielet positioning process as µ-transfer printing (µTP) or laser assisted mass tranfer (CLATT).
Here released coupons (chiplets/dielets) were released on a source wafer and transferred on a target wafer. An example of this approach is shown in Figure 5, which depicts the integration of an InP dielet used for laser integration in EPIC technology.
Here, the dielets consist only of a functional InP multi-quantum well material layer. After positioning the dielets and final structuring, common wiring layers (e.g., Al/W or Cu) are then implemented as part of a standard BEoL process continuation. As part of the QMI activities in WP1, these approaches are being further developed and used for the QMI of MEMS, RF, and CMOS components. The basic prerequisites for the development of these approaches are extremely accurate positioning of the chip and dielectrics on a target wafer.

QMI Integration of Chiplets

The surface quality of the target wafer and stable bonding processes are also essential here.

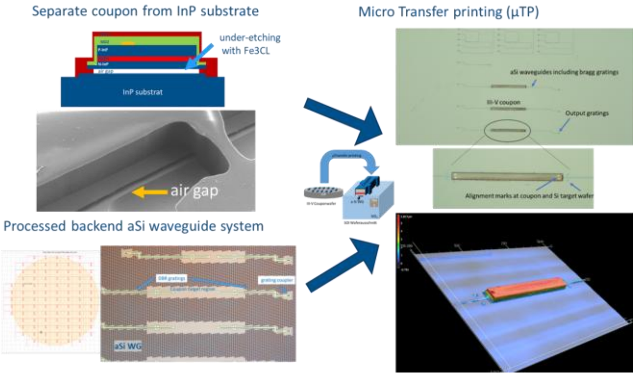

Figure 5: µTP process of InP coupon from a 3" source wafer to a SiO2 target surface on an 8" wafer (Source Leibniz IHP)

2.2 Module "Functional Interposers"

UHD Interposers

In this module the interposers to receive the individual components and chiplets will be built. As the various applications will provide different challenges, four main areas of R&D have been identified: ultra high density interposers, to address the need of HPC and AI system, Post CMOS interposers for RF/OPTO/MEMS to enable also non-digital applications, Passive functionalized interposers to allow the interposers itself to add value to the overall system and -not to the least- Organic interposers, which both form the bridge between advanced node based chiplets and the legacy devices including peripheral components.

The UHD Interposers have to ensure that even 2nm and below advanced node IC and chiplets with extremely small contact pitches and very high I/O counts can be merged on this first level of integration platform. This will require interconnect layers for micron scale I/O pitches using Backend of Line technologies. Thin film processes on 300mm wafer platform offering line/space capabilities in the 1µm regime (targeting 200nm by the end of the development of the APECS implementation) in combination with high aspect ratio Through Silicon Vias (TSV´s) of 20:1 for a TSV pitch offering to route 10^5 I/O per mm^2 from front to backside will address the challenges perceived for the 2nm node technologies. Anticipating a further reduction in the active node size (18A resp. 14A) will require I/O capabilities even higher than that – APECS will take up this challenge by researching 30nm scaled TSVs with ultrathin wafers.

Aside providing ultrahigh density interconnect basis for HPC and AI systems, interposers also play a crucial role in optical, RF and sensor platforms. Here, not always is silicon the material of choice. Ceramics and glass offer advantages in ambient resilience, RF performance and optical characteristics which make them especially suited for such applications. The core technologies to build onto these substrates, often at larger manufacturing dimensions than silicon (limited to 300mm diameter compared to 600x600 or even roll-to-toll), the fabrication of Through Vias, the filling of these and adding electrical routing is the common ground for all these interposers.

Non-Si Interposers

With glass for example, ultrasonic drilling, laser drilling, selective laser assisted etching are among the technologies used to realize holes at high density into the carrier, preventing the formation of micro-cracks in the amorphous material by properly tuning the process parameters. Filling of the vias, especially


Figure 4: TGVs formed via dual side (a and c) and single side (b) laser structuring. a) completely filled, b+c) conformally coated sidewalls; aspect ratio approx. 10:1, 470µm glass substrate

at high aspect ratios, faces the same challenges as seen with TSV´s albeit the typical geometries in glass are still larger (typ. 40..50µm) than in silicon (<10µm), see Figure 4).

Functionalized interposers

With a move away from passive nonfunctional interposers towards Si interposers with their own added functionalities, the possibility to add trench capacitances with high C values or even using post-CMOS interposers with a IC functionality on their own pave an additional pathway towards 3D functional integration.

Organic Interposers

Lastly, observing the need for high density substrates to interconnect 3D HDI modules to the next packaging level has spurred the development of "substrate like PCB" with high density via and routing layers. Such organic interposers, initially driven by the PCB industry, have seen a shift towards OSATs in the value chain, where substrates with fine line RDLs take up the challenge to sub-10µm L/S interconnect lines (Figure 6), offering also high aspect ratios to route multiple top layer routings to the backside for level 2 interconnects. Main challenges which have to be overcome here are the intrinsic instability of the organic material, which in contrast to

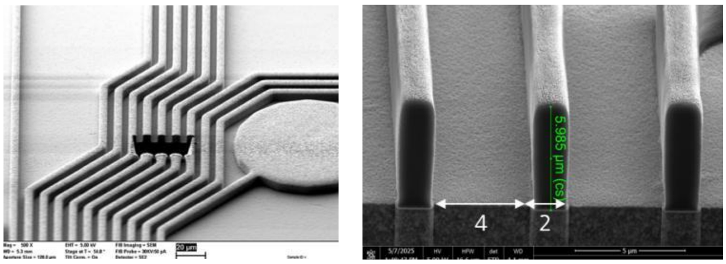

Figure 6: Fine-layer routing for advanced organic interposers

glass or silicon exhibits anisotropic behaviour and challenges with dimensional hysteresis during thermal processes

2.3 Module “Functional Integration”

Chiplets, but also standard IC components, are not inherently suited to be assembled onto the high-density interposers. Therefore, additional preparations are required to functionalize them for the next process steps. Here, depending on the intended integration APECS offers a number of approaches. The most straightforward one -and right now most looked after- is the deposition of multilayer barriers over the contact I/Os followed by the deposition of interconnect bumps. Depending on the targeted interconnect pitch, this can be micro-bumps for mass reflow, similar as known for the flip chip integration.

	WireBond	FlipChip	μFlipChip	μPillar FlipChip	Hybrid Bonding	Polymer Hybrid Bonding
Pitch (μm)	30	100	20	5	0,2	1
Interconnect Density (p.mm²)	10^1	10^1-10^2	10^3-10^4	10^4-10^5	>10^6	10^5-10^6
Interconnect process	sequentially	Parallel, Die	Parallel, Die	Parallel, Die	Parallel, Wafer	Parallel, Wafer
Infrastructure requirement	low	medium	medium	high	Very high	high
Cost	low	low	medium	high	Very high	high

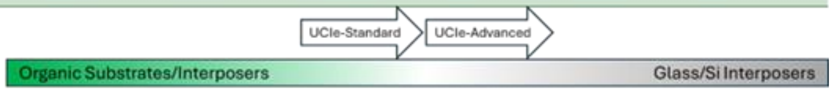

Figure 7: Comparison between different types of high-density interconnects, juxtaposed with target pitches according to UCIe standards

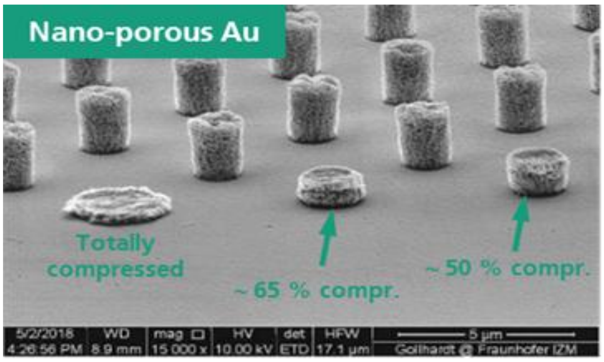

Figure 8: Au-nanosponge bumps for thermocompression bonding in the sub 10μm regime (compression stages indicated)

But with shrinking pitches, thermocompression and thermode bonding becomes the interconnect method of choice, allowing for sub 10μm interconnect pitches and below (Figure 8).

Chiplet Preparation

If even smaller, micron or even sub-micron interconnect pitches are required, hybrid bonding has since emerged – offering an even smaller I/O regime than the thermocompression method.

Either of the methods finds its use both in Die2Interposer assembly as well as in Wafer2Wafer Integration (Figure 7)

Aside from just providing the interconnect elements, also contact positions can be re-routed using thin film redistribution processes to allow for maximum compatibility of the system integration processes. Lastly, such thin film processes can also be used to add passive functionalities, i.e. resistors, capacitances and inductances to bring such elements closer to the point of use and remove the need for off-IC, larger peripheral components.

Especially for memory or -more generally speaking- chip(let) with similar functionalities that require scaling, 3D stacking has emerged as remedy to the footprint constraints modern systems face. Such processes have since been optimized for memory wafers leading to state of the art High Bandwidth Memory (HBM) cubes which stack up tp 16 layers of DRAM on top of each other (HBM4). While micro-bump interconnects on TSV´s are still state of the art, hybrid bonding of Wafer to Wafer offers an even higher degree of integration in 3D for the next generation of memory stacks.

3D Stacking

While inorganic hybrid bonding leveraging surface activation and recessed copper vias is currently the workhorse of industry, polymer assisted W2W bonding with deformable protruding metals (e.g. nanosponge or Al) offer advantages to the cleanroom ambient and process temperature and may be advantageous for a substantial number of applications aside from memory (Figure 9).

Not only wafer stacking, but also Die2Wafer integration benefits from the 3D stacking approach, especially when dissimilar chip(let) need to be integrated. Dissimilar I/O patterns can be adapted using advanced RDL technology (see previous section) to allow a perfect match for 3D stacking.

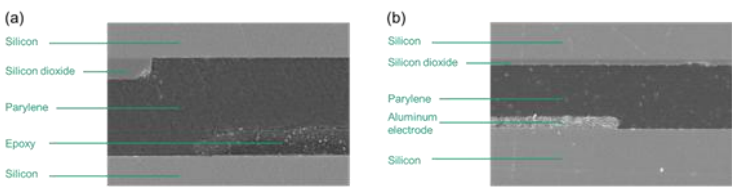

Figure 9: Parylene assisted hybrid bonding using Al contacts, showing the capability to compensate for surface recesses/imperfections (source: Fraunhofer ENAS)

Typically, a single IC or individual chiplet-function will not offer the full functionality required for a module. Supplemental IC or additional chiplets, complemented with passive components form such high-density modules (Figure 10) forming a System-in-Package (SiP).

Figure 10: Integrated module with HBM memory, passive devices and logic (source INTEL)

2.5D Integration

Integration of chiplets, complementary IC and passives on interposers ensures shortest interconnect pathways, thereby eliminating signal distortions and losses – thus interposers are core to accommodate a module´s functionality. As of such, using 3D stacks, side by side high density integration, adding passive functionalities (i.e. embedded capacitances or resistors) offer the realization of highly functional modules with minimum footprint.

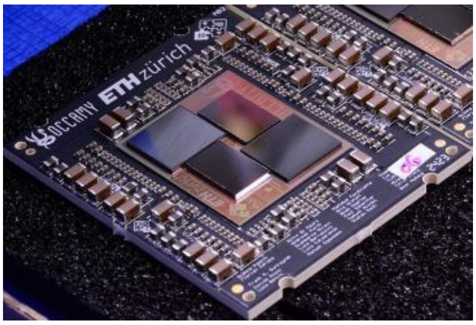

Figure 11: 2.5 D Integration of HBM stack & multi core chiplets on Si interposer on organic carrier substrate (source: ETH Zürich, Fraunhofer IZM)

Sometimes dubbed 2.5 D integration (mostly for side by side mounted IC or chiplets) or even 5.5D (in case multiple die-stacks are mounted together with side-by-side IC/chiplets), the preparation of wafer scale interposers in combination with high precision assembly and encapsulation technology is the hallmark of today´s capabilities in advanced packaging. (Figure 11).

Today´s technology focus is often limited to the digital world, as HPC and AI drive the advancement of IC and chiplet integration. However, analog functionalities, as being addressed also by the non-silicon based interposers, is a strong industry requirement as well. Ensuring process compatibility to the advanced IC integration, analog (sensor) packaging has to follow suit. Among these, recess-packaging to allow the integration of sensors in their working environment (i.e. vacuum, hermetic enclosure) is another aspect APECS is addressing, ensuring a full process chain for complex systems with external interface.

Sensor Integration

One activity here is the hermetic packaging of MEMS devices by making use of recessed glass interposers (Figure 12).

The processed developed as part of the module "Functional Interposer" seamlessly fits into this integration flow.

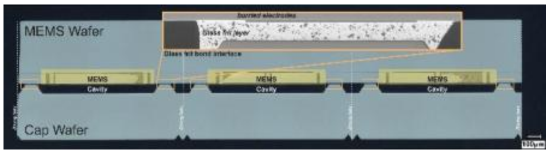

Figure 12:Recessed glass interposer packaging for MEMS devices (Source Fraunhofer ENAS)

2.4 Module "Advanced Packaging and Assembly"

Processes which address the realization of chiplet based subsystems are using capabilities stemming from semiconductor´s Backend-of-Line (BEoL) technologies, which inherently offer the micron scale integration.

However, such subsystems will have to be integrated also at a higher packaging level, posing unique challenges due to their fragile nature and -even at this expanded stage-minute contact geometries.

While on chiplet-interposer level, micron or even sub-micron features on flat, low TCE material dominate, at the higher packaging levels the I/Os have to match 10s of micron Line/Space limitations, warpage of the substrates, strong TCE mismatches and pattern registration issues.

Therefore, the APECS module on "HD Assembly of Modules and Subsystems" takes up this challenge, developing processes to cope with the large, warped and non-uniformly behaving system carriers.

HD Assembly

Such processes, however have to be conceptualized to not only address the integration issues, but also provide high speed assembly and should not incur a cost premium.

Solution approaches – among others- are e.g. adding another interposing layer to step in-between the high density contact arrangements of a Si interposer, compensating not only for the pitch-gap to the receiving substrate but also for TCE and coplanarity issues.

The "organic interposers", as described in the previous section, are excellently suited to address these challenges.

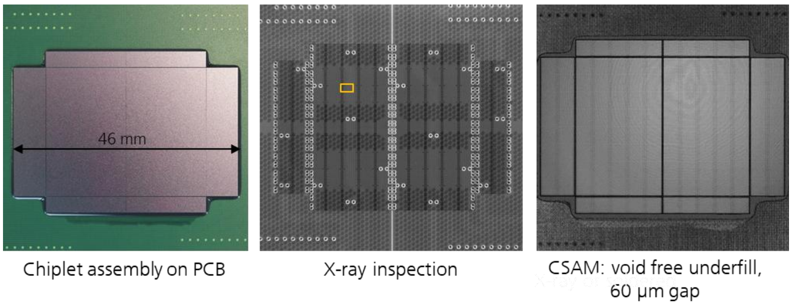

Figure 13:Example of in-process inspection to ensure quality

In-process monitoring along the entire process chain (e.g. Figure 13) and adapting process parameters "on the fly", not to the least using highly automated compensation methods with "Lot 1" process capabilities (i.e. screen printing plus local solder jetting) promise to cope with these challenges. Warpage compensation as early as design-in of compensation patterns, mechanical support bumps and simulation driven expansion compensation are other methods which have to be employed to ensure a successful process output and yield.
While Si or glass based interposers thus have their unique challenges, organic interposer technology using embedding or Fan Out processing offer a different take to the system integration. By dynamically adapting the routing pattern, processing deficiencies can be compensated while the system is built.
This -however- comes with an increased cost and new requirements for infrastructure and process capabilities. OSAT´s since have taken up this challenge and offer already System-in-Package solutions, which lend themselves more easily for the assembly to the motherboard. APECS is providing such capabilities for the smE and RTO partners as part of the module "Embedding Technology & FanOut System Integration (FO-SyI)" (Figure 14).

Fan Out System Integration

The combination of this FO-SI with the capabilities developed in the module "Functional Interposers" even promises an even higher degree of volumetric integration by stack laminating FO-SyI integrated panels (module "3D Layer Stack Assembly") with -as the APECS concept- four full panels of fan-out integrated sub-systems stacked layer-by-layer to form a 3D cube with unprecedented system functionality.

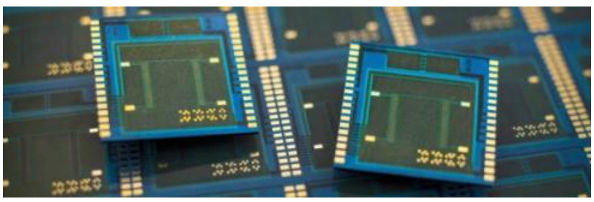

Figure 14: System scale integration using FanOut Panel Level Processes (source Fraunhofer IZM)

2.5 Interrelation between the modules

As the integration of chiplets into advanced packages and -finally- highly functional systems faces challenges all over the value chain, the technologies described have to be embedded into a holistic approach from Design to Qualification and Reliability assessment.

The paradigm of System-Technology-Co-Optimization (STCO) has since emerged, as the intertwining of the aspects creating the final system has -in contrast to the prior decades with a separation of the industries into IDM, OSAT and OEM- opened up more possibilities to realize a highly optimized system.
During design phase, for example, choice of optimum technology node for a specific application, the selection of interposer and interconnect processes, combined with in-process quality and performance analysis from the initial prototype feeding back into the cycle and allowing a (AI assisted) iteration towards an optimum, has hitherto not been possible to the extent that chiplets and the full range of integration in 2, 2.5 and 3D allows.
APECS therefore has established this STCO flow throughout its modules, with Design, Characterization, Testing and Reliability assessment an integral part of this methodology (q.v. Figure 1).

3 Summary

The APECS Pilot Line with its integration technology building block on 2.5 and 3D Integration addresses the challenges of all integration steps from the chiplet coming out of the fab to the fully integrated system.
This building block, consisting of advanced technology modules, combines Back-end-of-Line capabilities up to 300mm with panel scale integration processes for next generation interposers, the full chiplet preparation and integration process chain towards chiplet based System-in-Package and the system scale assembly and integration of such SiPs into fully integrated systems with unprecedented functional density.
Inter-module cooperation ensures that from design, fab-out, packaging and integration to -finally- verified system functionality and life time assurance, the STCO paradigm is seamlessly addressed to offer high performance, high reliability and low cost systems for the future application challenges.

4 Outlook

The APECS pilot line with its 2.5D&3D Integration focus is set into the context of Europe´s goal to set the stage for a global innovation ecosystem. The close collaboration with European RTOs as well as other pilot lines (i.e. WBG, Photonic, Quantum) will allow innovation synergies which hitherto have not been possible.

5 Acknowledgement

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6 Literature

"Nano-porous gold interconnect." , Oppermann, Hermann, et al. ,2010.DPC (2010): 002249-002290.
“Development of a Scalable AiP Module for mmWave 5G MIMO Applications Based on a Double Molded FOWLP Approach”, T. Braun et al.; 2021 IEEE 71st Electronic Components and Technology Conference (ECTC)

“Panel Level Packaging – Where are the Technology Limits?”, T. Braun; et al.; 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)
"Parylene as a novel packaging material for adhesive bonding, flexible electronics and wafer level packaging.", Selbmann, Franz, et al., 2024 IEEE 10th Electronics System-Integration Technology Conference (ESTC). IEEE, 2024.

"Adhesive-Free Bonding for Hetero-Integration of Inp Based Coupons Micro-Transfer Printed on Sio2 into Cmos Backend for Si Photonics Application on 8” Wafer Platform." Anand, Ketan, et al. , Available at SSRN 4702771.

"Key Technologies and Design Aspects for Wafer Level Packaging of High Performance Computing Modules.", Zoschke, Kai, et al., 2024 IEEE 74th Electronic Components and Technology Conference (ECTC). IEEE, 2024.

"Integration of III-V Components of 5G Transceiver in Embedding PCB-Based Technology.", Lim, Tekfouy, et al. 2024 IEEE 10th Electronics System-Integration Technology Conference (ESTC). IEEE, 2024.

"Development of an Adaptive Re-Distribution Patterning Process for Fan-Out Packages with Embedded High I/O Components.", Kahle, Ruben, et al., 2024 IEEE 10th Electronics System-Integration Technology Conference (ESTC). IEEE, 2024.