System-Technology-Co-Optimisation: The Heterogeneous Design Methodology in the APECS Pilot Line

Benjamin Prautsch[1], Elmar Herzer[1], Michael Mensing[2], Petra Künzel[3], Marco Dietz[4], André Lüdecke[5], Hendrik Boerma[6], Fabian Hopsch[1]
[1]Fraunhofer IIS, Erlangen and Dresden, Germany, {benjamin.prautsch;elmar.herzer;fabian.hopsch}@iis.fraunhofer.de
[2]Fraunhofer ISIT, Itzehoe, Germany, michael.mensing@isit.fraunhofer.de
[3]Fraunhofer ENAS, Chemnitz, Germany, petra.kuenzel@enas.fraunhofer.de
[4]Fraunhofer EMFT, München, Germany, marco.dietz@emft.fraunhofer.de
[5]Fraunhofer IMS, Duisburg, Germany, Andre.Luedecke@ims.fraunhofer.de
[6]Fraunhofer HHI, Berlin, Germany, hendrik.boerma@hhi.fraunhofer.de

Abstract

The chiplet era with advanced packaging calls for new heterogeneous design approaches. They must be able to combine different design domains across technological options while satisfying economic and performance demands from the application. It is crucial to ensure that the heterogeneous design meets the requirements with all relevant effects considered. Thus, a broad spectrum of information must be considered altogether. Such a holistic approach, however, has not yet been established to a significant extent. In the future, various chiplets and further components that are integrated into complex heterogeneous systems must be modelled, designed, simulated, analysed, and optimised in a comprehensive way and as simultaneously as possible. Among other topics, including quasi-monolithic integration (QMI), 2.5/3D integration, and characterization, test, and reliability (CTR), the APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems) pilot line will implement such an approach to cover a broad range from fundamental IC components, power management, compute units, and AI accelerators to various sensor implementations, and security features. Furthermore, different physical effects and couplings have to be addressed to meet a variety of analysis goals.
This requires a new and extended design approach: the *STCO design methodology* (STCO: System-Technology-Co-Optimisation), which is to be established together with industry partners as part of the APECS Pilot Line with associated standardization activities. It will capture, aggregate, and connect requirements, data, rules etc. to enable the monitoring and control of economic, technological, and design implications stemming from the components, packages, and chiplets that altogether form complex heterogeneous systems for various target applications. Various dependencies and feedback effects between design and the implications from the selected manufacturing technologies, as well as the reliability and environmental aspects are included. The STCO design methodology will also support the necessary connectivity to the European design platform, as it will make "From Lab to Fab" easier and more accessible for European companies, especially fabless SMEs, and academic institutions.

1 Introduction

Modern semiconductor components are becoming increasingly more complex and cost sensitive. To master technological and economic challenges, new chiplet approaches and heterogeneous integration technologies surge in demand. Accompanying this trend, advanced system design using pre-designed or custom building blocks emerges as one of the most differentiating performance enablers. While domain-specific design methodologies exist, to our knowledge, currently, no toolset and no workflow is capable to include the vast variety of existing and emerging semiconductor technologies. Thus, they are not sufficiently considered in modern System-Technology-Co-Optimisation (STCO) approaches and require domain-specific and cross-cutting human expertise.

1.1 Motivation of STCO Methodology for Chiplet Design

In chiplet-based system design, the proper selection of chiplet(s) and technology becomes imminent. This includes the choice to develop custom chiplet solutions or packages or reuse available technologies. To ascertain the possible benefits and additional cost of custom solutions requires significant effort. Often, non-existing chiplets require black-box estimations to evaluate their system-level benefit. Behavioural models are typically neither physically educated, nor accurate or account for interactions with other system level components. At this point, suitable STCO methodologies can guide the design effort and reduce overall cost by iteratively narrowing the chiplet requirements and behaviour expectations to benefit the application at hand.

1.2 State of the Art and STCO Accessibility

The System-Technology-Co-Optimisation design methodology is not new [1, 2, 3] but it is still in its infancy, as until recently, the design focus lied on monolithic system-on-chip (SoC) implementations. Without claims towards completeness, the following overview highlights STCO approaches and chiplet-based systems segmentations.
A study of recent advances and trends of chiplet design and heterogeneous integration is given in [4]. Among others, it discusses advantages and disadvantages of the chiplet approach, provides definitions, and gives real-world product insights into processor designs and an image sensor. It also covers various package integration technologies that were applied.

In [5], the chiplet approach is motivated based on computational demands, the slow-down of Moore's law, the lithographic reticle limit, and the ability to provide a broad portfolio of differentiated products while keeping the design efforts and costs manageable. The authors also emphasize the need for "silicon-package co-design" as a complete system in order to bring together planning, collaboration, engineering, and creativity. Furthermore, for two case studies, performance and costs are compared against each other and hypothetical monolithic integration.

In [6] and [7], the state of the art of chiplet-based integration is discussed while presenting initial generations of chiplet-based microprocessors. Another approach to heterogeneous 3D stacking for mobile products is presented in [8] where a base die in 22 nm and a compute die in 10 nm are contained. Besides briefly covering connectivity, thermal design, and test, also the need for CAD (computer-aided design) tools and system co-optimisation is briefly covered. Both internal and external CAD tools were enhanced to enable the 3D IC design by means of back-annotating 3D field solver results into the full-chip netlist.

A deeper consideration of the chip-package co-design problem is covered in [9]. There, a design platform is presented that addresses the hybrid design flow of both advanced packaging and chiplet integration.

For high frequencies, the simulation-based analysis of electrical signal transfer across components from different technologies is a must. This is especially used in millimetre wave applications like 5G or radar [10]. For proper operation after manufacturing, the analysis of the complete signal path from the transistor to the antenna is required. An ADK covering both the RF IC technology and an advanced integration technology enables this simulation, analysis, and optimisation.

Focusing on the architectural level, [11] proposes an automation approach that explores design partitioning into chiplets while evaluating cost metrics and inter-die communication as well as reuse across a family of products.

An observation is that as of now, STCO is not a state-of-the-art approach with ready-to-use CAD solutions. Often, it is rather an (at least partially) custom setup of various tools and flows that help to solve a specific heterogeneous design task for the target application. Key considerations here are costs and performance across a product family, while considering further aspects such as thermal, mechanical, yield, security & safety, and others.

1.3 Our Contribution

The APECS Pilot Line offers the unique opportunity to combine many domains and experts for heterogeneous integration. It ranges from *chiplet design* for digital, A/MS (analogue/mixed-signal), MEMS (micro-electro-mechanical systems), RF (radio frequency), and photonics over *advanced integration technologies* based on panel-level or wafer-level packaging to a range of *semiconductor technologies* from commercial ones to innovative, emerging materials like SiGe (silicon-germanium), SiC (silicon-carbide), III-V, or LNOI (lithium niobate-on-insulator). These are being processed in its extremes on 300 mm wafers in state-of-the-art semiconductor fabs and on die-substrates in university labs. This yields significant technological challenges in their integration into high-performance systems. Originating from this opportunity, the APECS Pilot Line envisages to establish and embed a domain-independent, holistic STCO workflow with well-defined technology partitioning and interfaces into the European semiconductor ecosystem. In this special session paper, we describe the STCO approach, cover our STCO workflow, present related challenges, and discuss domain-specific STCO flows.

2 Problem definition of Heterogeneous Chiplet Design

Heterogeneous chiplet design starts out with a functional view and breaks it down to an optimal mixture of often incompatible semiconductor technologies with different design rules and tools. As such, the well-defined IP-driven ecosystem is not capable to capture all design challenges and elaborate multi-physics simulations in one tool. For instance, chiplet-scale mechanical or (electro-)thermal simulations are required for functional optimisation. Therefore, an STCO methodology is necessary to combine the variety of data and domains like design sources, IPs, design methods, integration steps, economic and ecologic constraints, and process details into a holistic system design approach across the hierarchy levels of the system (**Figure 1**).

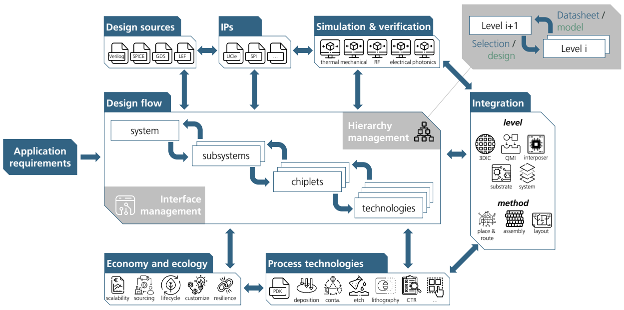

Figure 1 Schematic STCO dependency overview

2.1 Prerequisites for STCO CAD

In order to optimise a heterogeneous chiplet implementation, trade-offs between possible product performances and costs must be investigated across process technologies. Thus, various physical domains, dependencies, and details must be handled simultaneously. To gain such insights by computer-aided design, a common database with systematic data entry and access levels is an essential prerequisite. This database must feed a central STCO tool which interacts with a spectrum of people and/or software tools such that an overall optimisation of system and technology can take place. It must cover both the cost aspects and the technical aspects. Thus, it should provide relevant key figures from component datasheets, technology information, information across technical abstraction levels, and from various domains (electrical, security, geometric, thermal etc.). Important data to be available includes requirements, interface definitions, ready-to-use PDK/ADK (process design kit/assembly design kit), and use case scenarios. Thereby, STCO should not replace but complement and connect design tools by unified data formats and interfaces.

2.2 A Large Variety of Technologies and Technical Domains

Semiconductor technologies enable wide range of functionalities, including digital, A/MS, MEMS, RF, and photonics. Chiplet architectures and heterogenous integration provide novel system designs by bringing together multiple chiplets of similar functionality or by combining multiple functionalities into one chiplet module. These two scenarios are considered in the following.

2.2.1 Multiple Chiplets with Similar Functionalities

Modelling of systems with similar functionalities can likely be handled in one tool. Decisions on architectural level include dividing functionalities into multiple chiplets, selecting the interconnection technology, and determining the optimal chiplet technology itself. In some cases, a monolithic integrated system might even be advantageous for the overall system regarding performance and cost.

2.2.2 Systems with Diverse Functionalities from Multiple Physical Domains

System design where diverse functionalities from multiple domains are combined is challenging because design, simulation, operating modes, and modelling tools often differ greatly. Currently, it is not feasible to design most combinations of these functionalities in one single tool. Thus, STCO needs generic models of mutual influences between the chiplets and interconnects to estimate the system performance. A generic parent system model might be used to find the optimal technology mix for the desired system, while more specialised models are considered for the optimisation of the individual chiplets and interconnects.

To refine and improve all models, a broad spectrum of characterization and measurement efforts should be conducted for each semiconductor and interconnection technology. Data transfer between the different technologies should be considered in the STCO approach as well.

3 APECS' STCO Design Methodology in General

Figure 2 presents an overview of the process to implement a chiplet module from the customer's requirements. For the sake of clarity, in this paper, the "chiplet module" sketched on the upper right of the figure is a representation of a heterogenous integrated (sub)system we focus on. Such chiplet module is built out of chiplets and an (advanced) "substrate" which can be any interposer and/or substrate using a variety of technology options.

The design phase evaluates decisions on how to partition the system into chiplets and likewise the chiplets internally. Thereby, the functional interactions must be considered while handling various physical effects (electrical, mechanical, thermal, optical, etc.) which depend on the technologies. Based on this, the design of the chiplets, substrate, and chiplet module can be executed to finally generate production data. To accomplish this, more input is needed as indicated by arrows at the top of **Figure 2**.

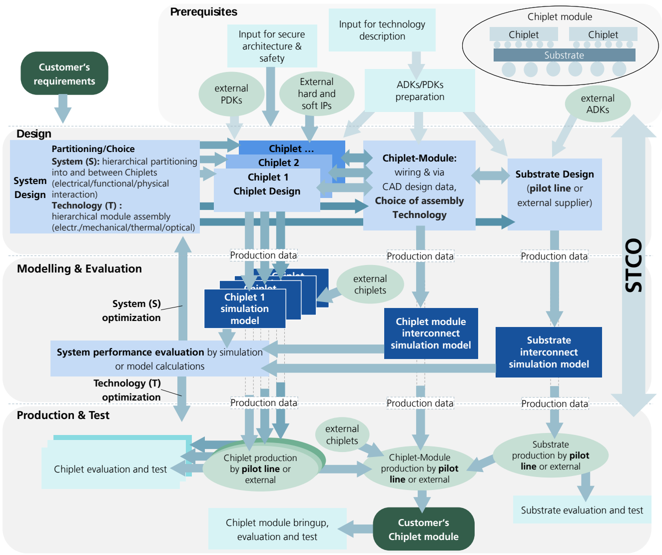

Figure 2 Path from the customer's requirements of a system to a chiplet module using the STCO methodology in the scope of the APECS Pilot Line

From the production data, models are derived which are used to estimate the system performance to be verified against the specification. When the specification is not met, there is a loop back to system design and/or the technology to change or adjust parts of the system decisions and/or the technology until the module reaches satisfactory performance. This iterative approach is the core of STCO. It intends to answer the following questions:

- *Which components* from *which (optimal) technologies* are necessary to fulfil the requirements?
- Into *how many chiplets* should the module be divided?
- *Which integration/interconnection* approach is needed?
- What are the *key performance indicators* (*KPIs;* area, costs, performance, …)? Which are the degrees of freedom of the decisions to take influence? How sensitive is the outcome to changes? Is there a continuous design space or are only discrete selections possible?
- What is an adequate choice of *signal interfaces* (electrical, optical, mechanical, …)? How can the interface selection manage communication challenges like bandwidth or signal integrity and which implication has this choice to other parts of the system?
- How is *power delivery* implemented?
- Are there *more challenges* to be considered like thermal, mechanical, or electro-magnetic interference?
- Which additional parts in the system and which additional procedures while manufacturing are needed to obtain *testability* for all parts and/or the whole system (Build-In-Self-Test, test bumps, …)?
- What are the *costs*, considering test costs, design costs, reuse, etc. and what is the yield of the solution?
- Is there a reliable *supply chain* for the selected technology (or access at all)?

The number of iterations needed depends on the quality of the input data (e.g. A/PDK) compared to the requirements to be achieved. There might be no loop needed in case all sub-design tasks can provide correct submodule performances that add up to the correct system performance.

3.1 (Our) Definition of STCO

The term STCO is still emerging. In [1] and [2], STCO bridges the gap between application-driven systems and technology which extends design technology co-optimization (DTCO). What a "system" is, however, often depends on the individual view and broader context. We focus on chiplet modules (see above) which can be used as part of a larger piece of hardware solution (i.e. as a subsystem) together with, e.g., a PCB (printed circuit board) carrier and further components.

Our STCO approach targets the optimal realization of a chiplet module regarding both application requirements (use case) and economic goals (business case). The use case breaks down into a variety of more specific requirements across multiple technical domains, including technological, electrical, geometrical, mechanical, optical, interfacing, thermal, reliability, and safety & security aspects. On the business case side, costs and efforts regarding design, manufacturing/yield, licenses, 3rd party components, reusability, and others must be considered to provide benefits across products and/or product families for both the solution provider and their customers. With STCO, this diverse landscape of options across domains is systematised and quantised such that techno-economic decisions can be taken fast and holistically.

3.2 The Relevance of Modelling

To enable the iterative bottom-up paths in **Figure 1** and **Figure 2**, later steps in the design flow must be anticipated early. Furthermore, the various physical domains have to be considered simultaneously. This necessitates various models which provide the relevant information. To anticipate the relevant information across requirements (e.g., performance, costs, geometry, supply, etc.) and design hierarchies, both a well-informed database and a spectrum of models are required that replicate the lower-level details to support the broader view of system optimisation.

3.3 Design Tool Ecosystem

As shown in **Figure 1**, a successful STCO design flow depends heavily on a variety of design data, such as PDKs, design IPs, and verification models, that are available for various process technologies. This data is typically provided for established design tools, which must then be used in the design flow for the technologies selected. When using complementary metal-oxide-semiconductor (CMOS) technology for the design of microelectronic circuits, only commercial tools from leading electronic design automation (EDA) providers are typically supported first – or at all. However, there are some CMOS technologies that support a design flow with open-source design tools [12, 13]. The EU promotes the dissemination and use of open-source design tools, and the various PDKs and ADKs created in APECS will also support open-source tools.

The design tools for chiplet design offered by commercial providers often focus more on the design flow of digital circuits, especially for high-performance computing (HPC), as this has been one of the main areas of application for chiplets in the past. In addition to digital design, APECS will also provide complex analogue circuits and a range of other technologies for the integration of additional physical domains (mechanical, photonic, acoustic) for the construction of complex sensor and actuator chiplets. Each of these domains uses domain-specific design tools (e.g., domain-specific finite element method (FEM) simulators), which must also be integrated into the STCO design flow as part of PDK and ADK development. Due to this variety of tools used, it is necessary to repeatedly synchronise the domain-specific design processes in the overall design flow. Typically, the verification steps in the design flow are suitable for this purpose, also from a tool perspective. By providing suitable common simulation models at different levels of abstraction (e.g., Universal Verification Methodology (UVM), transaction level models, S-parameter models in SPICE, real number models in SystemVerilog, etc.), the overall system can be verified in the different design phases. The layout and physical verification also works well as a synchronization point for domain-specific flows, since GDSII (Graphic Design System) is an exchange format supported by commercial and open-source layout tools as well as by verification tools. Furthermore, the necessary assembly and interconnect rules must be integrated into the domain-specific design flows as additional rules. The physical layout verifications required for this can be carried out jointly across technologies by transferring the most important design layers (interconnect and pad layers) to a common PDK/ADK and extending the respective design rules accordingly. Also, the electrical, thermal, and mechanical (parasitic) effects, which must be considered due to the interconnects to the respective substrate (interposer, package, circuit board), must be transferred from the PCB tools to the IC simulation models so that they can be considered early in the design flow.

3.4 Pathways to an STCO Reference Flow and its Dependencies

In APECS, a variety of technologies is combined. To address use cases out of this spectrum, the general STCO design flow must be augmented by the technology details. At the same time, the design process must be represented in a holistic way to connect the domains. This enables to keep the overview and aggregate global KPIs when simultaneously designing the system and refining the technologies. Following, a summary of STCO activities and peculiarities is given for different chiplet domains beyond digital and A/MS.

3.4.1 STCO for MEMS

Micro-electro-mechanical systems comprise a large variety of functioning principles resulting in a broad variety of fabrication technologies [14]. Their accompanying electronics are usually implemented in a CMOS technology, but also additional discrete elements are used to build custom sensor systems. The large variety of physical domains, the sensors are working in, combined with their respective technologies demands for a multi-domain design flow for design and verification.

In general, the design can be distinguished into a *layout-focused approach* and a *model-focused approach*. In the *layout-focused approach*, relevant details are captured in a GDSII layout. Models for multi-physics simulations are derived from this layout, as well as the sensor specification and abstract behavioural models for the usage in, e.g., circuit simulators. This approach has the advantage that layout checks for fabrication feasibility are possible with a design rule check at each design step, as existing PDKs can be used. The workflow can be modularised with different design tools like commercial design tools for CMOS development and layout, open-source tools for specialised layouts, and open source or commercial FEM tools for the multi-domain analysis. The *model-focused approach* puts more emphasis on the system development involving a "digital twin" and the layout is derived from the model. This requires more complex model interactions and a workflow which integrates all functionalities seamlessly but can lead to more powerful models.

For a successful STCO design, the interfaces between all design levels need to be specified and wrapped for the usage in different tools. Electronics and packaging may influence the operation of MEMS systems. Therefore, cross-domain abstract behavioural models of the MEMS need to be derived. The ADK addresses specific boundary conditions of a certain chiplet like thermo-mechanical and electrical requirements and possible follow-up technologies.

3.4.2 STCO for Photonics

In quasi-monolithic photonic integrated circuits (PICs), the photonic process layers are deposited on finished CMOS wafers (post-CMOS) [15]. Alternatively, PICs can be monolithically integrated in III-V or LNOI wafers, and e.g. hybridly or heterogeneously integrated with high-speed electronics on an interposer [16]. For the former case, the control electronics for the photonic components are partially implemented in the CMOS part of the chiplets. For the latter case, interconnects are co-designed between different technologies. For both cases, the close interaction between the microelectronic and photonic subsystems in such electronic-photonic co-integration requires a multi-domain design flow. In addition to the use of commercial design tools for CMOS circuit development, open-source EDA tools are to be used for the development of photonic structures.

For successful STCO design of PIC chiplets, the ability to verify the system at all design levels using cross-domain simulations is crucial. To achieve this, verification models are being developed at different levels of abstraction, which can be used in various simulators, including open-source simulators. The use of open-source layout tools is also an important part in the design flow. They offer the possibility of creating photonic structures via the GDSII exchange format and verifying them together with the interconnect layers. Furthermore, the assembly of PIC chiplets requires additional adjustments in the PDK of the technologies involved. For example, the design rules of the PDKs must be extended to include additional assembly rules, due to the necessary optical coupling. Since no technology is optimally suited for all applications [16], a multi-domain approach for the integration of photonic chiplets into a system is essential to optimise the overall system's KPIs.

3.4.3 STCO for Power

Power electronic system design and optimisation is an example of an application area that already relies on optimisation techniques to meet modern performance, efficiency and cost requirements. The optimisation effort is performed in a highly partitioned ecosystem across the domains power discrete devices or components [17], modules [18, 19], and systems [20]. Power management ICs and monolithic integrated power electronic solutions commonly bridge the domains and have similarities to analogue and RF design methodologies, while continuously balancing higher abstraction levels with better accuracies of the utilised models.

For power discrete design, emphasis is given on the optimisation and balancing of different device regions (i.e. core and termination structures) as well as interconnect parasitics. Based on these active device layouts, specialised, predominantly commercial tools emerged that allow for routing optimisations with respect to resistance and current density distributions, which are critical for wide bandgap semiconductors that allow for high current densities and switching frequencies. The optimisation of power discretes towards system level performance, mixed-mode (TCAD and SPICE) or purely compact model-based approaches are utilised.

Assuming a (packaged) power discrete, designers create power modules using a workflow starting with schematic design and circuit simulations (e.g., SPICE, VHDL). Note that sourcing could in practice also include bare-die power chiplets. However, typically the discrete design space is limited to component selection, not including modifications on power discrete level, due to the complexity and economics of power discrete development and manufacturing. Continuing from the circuit simulations, FEM tools are used for physical prototyping and to optimise the placement and routing within the power module. In advanced workflows; the FEM tools feature integrated interfaces to circuit simulators allowing for automated feedback loops.

For power systems design, power modules or packaged discretes (and driver ICs) are included in system level circuit simulators similarly to the previous abstraction level via behavioural models, or additionally, by simplified compact models. Likewise, the optimisation of placement of components and routing between components is performed using board-level EDA tools and, if required, by FEM simulators.

While this segmented development approach has well defined interfaces, it inherently limits the potential for system level co-optimisation in power electronics.

3.4.4 STCO for RF

When radio frequency-related chiplets are designed by STCO, there are some additional challenges to solve. Additional information is necessary from the ADK, provided formats for models into the STCO is required, and the interaction between RF chiplets and other system parts by unwanted coupling must be quantifiably to both measure and counteract this. In particular, the 3D interconnects between RF chiplets as well as to other chiplets place new and special demands on STCO, as they become essential in 2.5/3D heterogenous integrated modules and systems. This is due to the individual design of the interconnects. To enable STCO for RF, there must be some degree of freedom for modification from the system side and also from the technology side. This could be different options of materials, that are analysed using the ADK and evaluated according to the requirements for the application, so that the result of the STCO is an optimised system.

While the ADK and the models it contains must be expanded, new approaches must be established for the 3D connection of RF chiplets to each other and to other chiplets in the STCO. The special challenges compared to analogue design, for example, are that traditional RF chip design usually requires co-simulations with electromagnetic (EM) solvers in addition to SPICE-related circuit design. This is necessary to precisely consider parasitics for very high frequencies on the one hand and to create precise models for the individual passive structures and components in the RF domain on the other. For 2.5/3D heterogenous integration, furthermore, synthesis tools are necessary to effectively design the 2.5/3D passive structures. Part of these tools are optimisation algorithms to find the optimal solution regarding predefined parameters like size and performance within the design rules. For STCO, all the aforementioned tools and solvers have to be anchored in an overarching design flow. Cross-coupling must also be part of the STCO process in order to ensure valid functioning of integrated systems.

4 Conclusion and Outlook

System-Technology-Co-Optimisation (STCO) will be an enabler to realise tailored chiplet modules that simultaneously meet cost, performance, and reuse requirements of various target applications. For this, it is necessary to combine a broad spectrum of technical domains and experts to design and manufacture such optimised chiplet modules that are built out of a well-arranged mix of physical considerations and technological options.

Still, there is a long path to go in order to reach this vision of a unified design platform that combines the various use cases and commercial needs. In this paper, we presented the related challenges, dependencies, and sketched STCO pathways. In order to bring together the relevant industries from application, technology, design, and CAD, the industry will have to collaborate closely and define standards to enable this new quality of cross-domain exchange and collaboration.

5 Acknowledgement

The work presented was carried out in the framework of the APECS Pilot Line of the Chips Joint Undertaking, funded by Horizon Europe (ID: 101183307) and Digital Europe (ID: 101182906) Programmes and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain. .

6 Literature

[1] S. Pal, A. Mallik and P. Gupta, "System-technology co-optimization for advanced integration," *Nature Reviews Electrical Engineering*, p. 569–580, Sept. 2024, doi: 10.1038/s44287-024-00078-x.

[2] L. M. G. Rocha, M. Naeim, G. Paim, M. Brunion, P. Venugopal, D. Milojevic, J. Myers, M. Badaroglu, M. Verhelst, J. Ryckaert and D. Biswas, "System-Technology Co-Optimization for Dense Edge Architectures Using 3-D Integration and Nonvolatile Memory," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, no. 10, pp. 125-134, 2024, doi: 10.1109/JXCDC.2024.3496118.

[3] J. D. Boeck, J.-R. Lèquepeys and C. Kutter, "1.3 EU Ships Act Drives Pan-European Full-Stack Innovation Partnerships," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 26-32, 2023, doi: 10.1109/ISSCC42615.2023.10067442.

[4] J. H. Lau, "State-of-the-Art and Outlooks of Chiplets Heterogeneous Integration and Hybrid Bonding," *International Microelectronics Assembly and Packaging Society*, pp. 145-160, 2021, doi:10.4071/imaps.1542066.

[5] S. Naffziger, N. Beck, T. Burd, K. Lepak, G. H. Loh and M. Subramony, "Pioneering Chiplet Technology and Design for the AMD EPYC™ and Ryzen™ Processor Families : Industrial Product," *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA)*, pp. 57-70, 2021, doi: 10.1109/ISCA52012.2021.00014.

[6] G. H. Loh, S. Naffziger and K. Lepak, "Understanding Chiplets Today to Anticipate Future Integration Opportunities and Limits," *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 142-145, 2021, doi: 10.23919/DATE51398.2021.9474021.

[7] G. H. Loh and R. Swaminathan, "The Next Era for Chiplet Innovation," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 1-6, 2023, doi: 10.23919/DATE56975.2023.10137172.

[8] W. Gomes, S. Khushu, D. B. Ingerly, P. N. Stover, N. I. Chowdhury and F. O'Mahony, "8.1 Lakefield and Mobility Compute: A 3D Stacked 10nm and 22FFL Hybrid Processor System in 12×12mm2, 1mm Package-on-Package," *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, pp. 144-146, 2020, doi: 10.1109/ISSCC19947.2020.9062957.

[9] L. Cao, C.-C. Wang, C.-Y. Huang and H.-C. Kou, "Advanced Packaging Design Platform for Chiplets and Heterogeneous Integration," *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, pp. 1032-1037, 2023, doi: 10.1109/ECTC51909.2023.00176.

[10] F. Hopsch and A. Heinig, *A reference flow for chip-package co-design for 5G-mm-wave using Assembly Design Kit (ADK)*, Online, 2021.

[11] A. Sangiovanni-Vincentelli, Z. Liang, Z. Zhou and J. Zhang, "Automated Design of Chiplets," *In Proceedings of the 2023 International Symposium on Physical Design (ISPD '23)*, pp. 1-8, 2023, doi: 10.1145/3569052.3578917.

[12] S. Ortega-Cisneros, E. I. Baungarten Leon and P. Mejia-Alvarez, Integrated Circuit Design - Tape-out Process with Open-Source Tools, Springer Cham, 2025, doi: 10.1007/978-3-031-92108-7.

[13] "Open Source PDK in 130nm BiCMOS, developed for Analog/Digital, Mixed Signal and RF ASIC Design," Leibniz Institute for High Performance Microelectronics, [Online]. Available: https://www.ihp-microelectronics.com/services/research-and-prototyping-service/fast-design-enablement/open-source-pdk. [Accessed 1 August 2025].

[14] A. S. Algamili, M. H. M. Khir, J. O. Dennis, A. Y. Ahmed, S. S. Alabsi, S. S. Ba Hashwan and M. M. Junaid, "A Review of Actuation and Sensing Mechanisms in MEMS-Based Sensor Devices," *Nanoscale Research Letters*, vol. 16, no. 16, Jan. 2021, doi: 10.1186/s11671-021-03481-7.

[15] M. Westhues, T. Geruschke, J. Hauser, R. Burkard, A. Nesic and A. L. Schall-Giesecke, "Highly Flexible Dielectric Platform for Post-CMOS Photonics," *The 25th European Conference on Integrated Optics (ECIO 2024)*, vol. 402, 2024, doi: 10.1007/978-3-031-63378-2_96.

[16] P. Kaur, A. Boes, G. Ren, T. G. Nguyen, G. Roelkens and A. Mitchell, "Hybrid and heterogeneous photonic integration," *APL Photonics*, vol. 6, no. 6, 2021, doi: 10.1063/5.0052700.

[17] P.-J. Chuang, A. Saadat, S. Ghazvini, H. Edwards and W. G. Vandenberghe, "Constrained Bayesian optimization using a Lagrange multiplier applied to power transistor design," *Journal of Computational Electronics*, no. 5, 2025, doi: 10.1007/s10825-025-02356-9.

[18] A. I. Emon, H. Carlton, J. Harris, A. Krone, M. U. Hassan, A. B. Mirza, M. Hossain, A. U. Rashid, Y. Chen, F. Luo, D. Huitink and A. Mantooth, "Design and Optimization of Gate Driver Integrated Multichip 3-D GaN Power Module," *IEEE Transactions on Transportation Electrification*, vol. 8, no. 4, pp. 4391-4407, Dec. 2022, doi: 10.1109/TTE.2022.3173585.

[19] E. Persson, "Optimizing PCB Layout for HV GaN Power Transistors," *IEEE Power Electronics Magazine*, vol. 10, no. 2, pp. 65-78, June 2023, doi: 10.1109/MPEL.2023.3275311.

[20] H. Rasool, B. Verbrugge, A. Zhaksylyk, T. M. Tran, M. E. Baghdadi, T. Geury and O. Hegazy, "Design Optimization and Electro-Thermal Modeling of an Off-Board Charging System for Electric Bus Applications," *IEEE Access*, vol. 9, pp. 84501-84519, 2021, doi: 10.1109/ACCESS.2021.3086392.