APECS

Coordinated by Fraunhofer

Implemented by Forschungsfabrik Mikroelektronik Deutschland

Joint Technology Development by imec and Fraunhofer ENAS, IMWS & IZM

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Work Package Overview

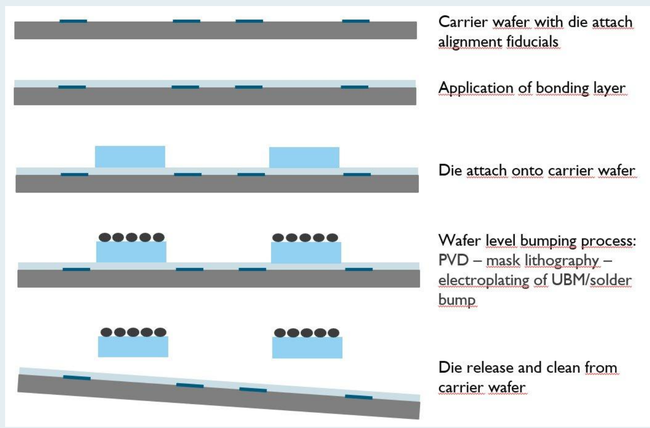
The two institutions involved in this topic, imec and FMD, have the needed infrastructure, employing complementary technology building blocks, i.e. RDL, 3D stacking and overmold vs. singulated chiplet µ-bumping, 2.5D assembly, molding and packaging. The study will cover a variation of chiplet size and interconnect density. The primary objective is to assess the technological capabilities to be engaged for an EU cooperation pilot line.

The process starts with the RDL 1st realization on a carrier wafer, the chiplet assembly is done (featuring a mix of bump pitches of 40µm, 50µm and 100µm) at both RTO sites with different die thicknesses. Molding is carried out afterwards, whereas the mold cap is thinned down until revealing chiplet back sides. After carrier release, balling and board assembly is done. To optimize the performance of the package, test chips are developed (with integrated heater, temperature sensor, stress sensor, humidity sensor), that can simulate different heating schemes (heat spots or large heat surfaces) and new thermal management concepts will be integrated (SiC as heat spreader, 3D printed fluidic heat dissipation systems).

FMD will support the process development by advanced failure analysis to identify process related defects and related failure modes and to adapt innovative defect metrology and analysis methods for novel key technologies like imec´s backside power delivery ICs, hybrid bonding, advanced RDL and 3D packaging to support and speed up technology qualification and ramp up. This includes the development of design for failure analysis concepts to enable more efficient and quantified localization of electrical defects within the complex 3D electrical routing of high-performance SiP. The module assembly process flow will be digitized by FMD as a compact digital twin model for virtual process and reliability optimization.

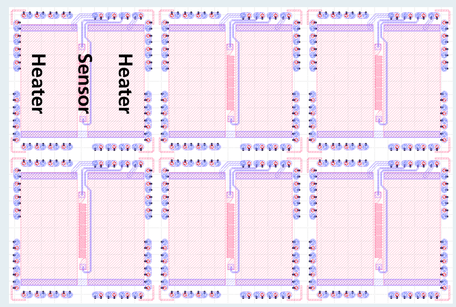
To enable access to the pilot line even with chiplets from multi project wafer runs that have no bumping, Fraunhofer IZM will enhance their single chip bumping capabilities. Concept on FhG side is ready, manufacturing will start beginning of 2026, but the overall process is waiting until end of 2026 for installation of high precision D2W die attach placer (IZM-002.1).

Single Chip Bumping

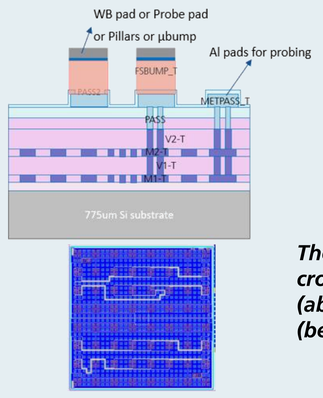


For thermal analysis test chiplets are developed, especially to study the behavior of heat spreaders attached to ´the top side of the package. For that, imec is developing a thermal test die that can be integrated on the RDL interposer with very small heating spots that are also used as a calibration device for the lock-in thermography done at FhG IMWS. In contrary, FhG IZM will develop a thermo-/humidity-test chiplet with larger heating areas and higher wattage output that can be used in a more general fashion (pixelated heating chiplets can be combined in different die sizes) to study heat spreading in FOWLP.

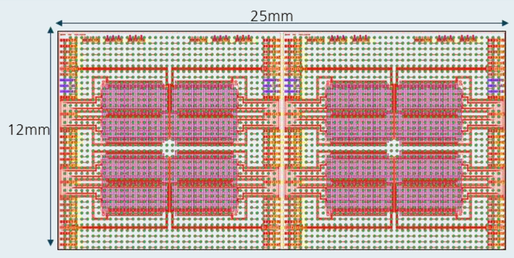
Thermo-/Humidity-Test Chiplets

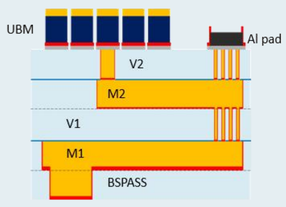


Thermal chip (top die) and RDL interposer Design



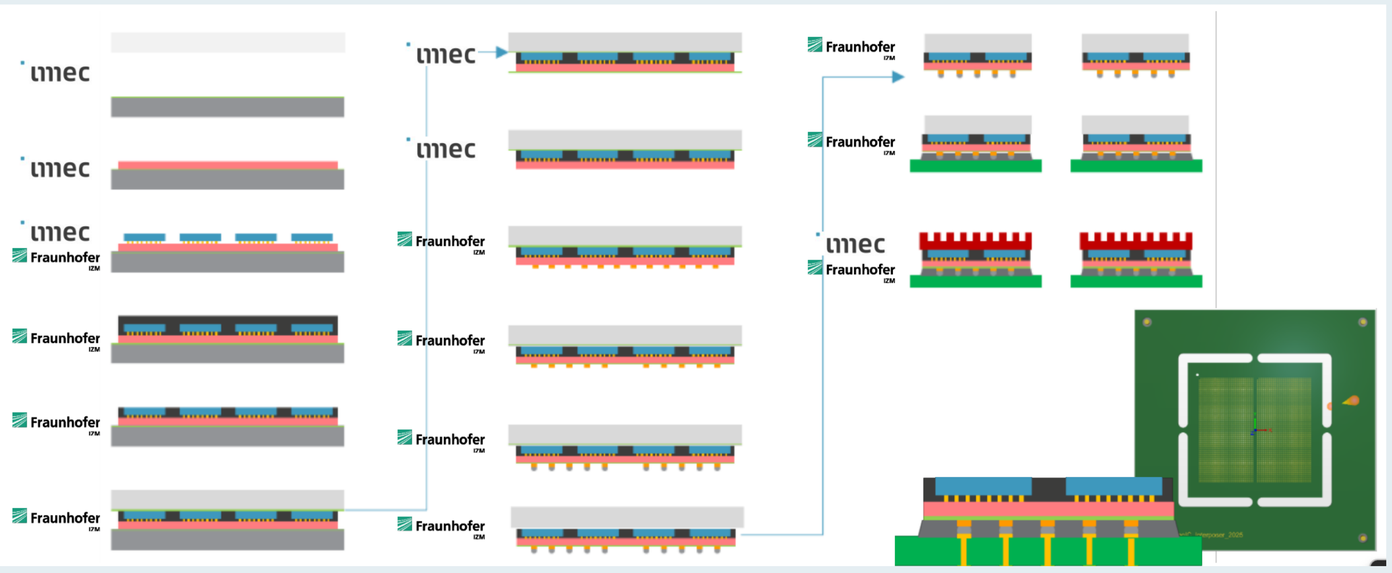
Thermal chip (top die) cross section view (above) and top view (below)





RDL interposer top view (above) and cross section view (below)

RDL 1st FOWLP - Process Flow Overview



Summary

- RDL 1st Packaging Demonstrator process flow is established, starting with several short loop runs between imec an dFhG IZM
- Thermal lock-in thermography is available at FhG IMWS, stackable thermo-test chips for calibration are in the design flow at imec
- Single chip bumping process concept is ready at FhG IZM, processing starts in 2026
- Thermo-/Humidity-test chips for package test are designed at FhG IZM and first samples are manufactured in 2026
- Digital Twin analysis are starting at FhG ENAS in 2026

Joint Technology Development

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Additional information

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