APECS

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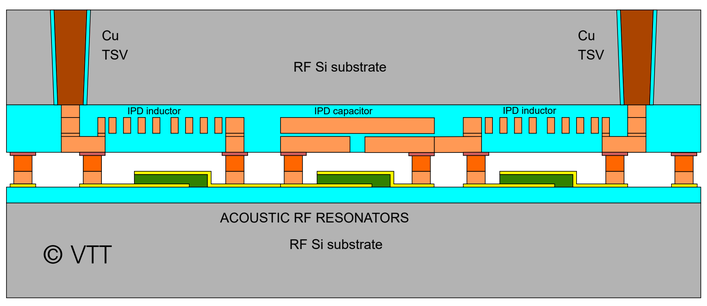
The objective of task 5.4 is to develop and demonstrate wafer-level packaging and integration technologies for RF (6G) and optical (VIS-NIR) applications. RF application will be the demonstrator radio front end module consisting of active IC components and BAW filters from Fames pilot line, integrated with APECS technologies including, antenna, waveguides, IPDs and interposer / integration / packaging. The optical application will be packaged MEMS Fabry-Perot interferometer (FPI). Both TGV and TSV technologies will be applied, with the target to utilize ALD technologies in TSV fabrication. Additionally, panel-level LTCC packaging capabilities will be developed and demonstrated with RF devices.

IPD and RF on Si and glass substrates

The main objective is co-design and hybridization of RF BAW filters and IPDs at 7 – 15 GHz following Si-Si and Si-glass BAW-IPD technology approaches. Combining BAW and IPD allows use of advanced synthesis methods in filter design, enhance BAW resonator coupling and filter bandwidth, and uses IPD elements as an impedance matching circuit for the filter. Bonded Si-Si or Si-Glass wafers act as a self-packaged module.



IPD-BAW module concept using Si-Si bonding technology with copper TSVs

ALD for TSV

For high aspect ratio vias the challenge of coating a conformal pin-hole free barrier and seed layer for the subsequent electrochemical deposition (ECD) of copper is addressed by atomic layer deposition (ALD) and compared against chemical vapor deposition (CVD) approach. TSV's with aspect ratio around 12:1 are demonstrated with an ALD based TiN barrier and ruthenium seed layers by VTT and FhG. Additional Co ALD and Cu CVD are used for comparison with the ALD films.

Work includes the implementation of metallization layers via damascene processing to produce the needed interconnects for routing in heterogenous integration for enhanced 2D and 3D integration by VTT. Both VTT and FhG implement material characterization techniques to benchmark the combination of materials among each other and to inform future PDK development. ECD process implementation for interlayer vias, interconnect lines and TSV's with parallel ECD process modelling supports implementation of digital twins and PDK development. The sum added value of the package seeks to brings within both VTT and FhG a scalable TSV process for heterogeneous and advanced packaging technology bringing a swath of opportunities for piloting activities.

IPD design for 160GHz Technology Demonstrator

The main objective of this work is to develop Integrated Passive Devices (IPDs) suitable for D-Band applications. The focus will be on the design, simulation, fabrication, and characterization of key passive components, including filters, resistors, and capacitors, implemented on glass wafers. Glass is chosen as the substrate material due to its low loss, high resistivity, and excellent suitability for high-frequency and high-density integration. Different layout strategies and material parameters will be evaluated. Measurements will be carried out to validate the electrical performance of the components and to compare the results with the simulation data.

160GHz Technology Demonstrator

The developed IPDs will then be integrated into a D-Band demonstrator implemented on a glass interposer. This demonstrator will combine the IPDs with an active Power Amplifier and a substrate integrated antenna using TGVs as a conductive element. The overall system will be measured to verify the performance of the IPDs in a realistic operating environment and to assess their impact on the link budget and radiation characteristics. The results will demonstrate the feasibility and advantages of glass-based IPD technology for future D-Band communication and sensing applications.

Glass interposer with TGVs and multi-layer RDL with assembled test chiplets
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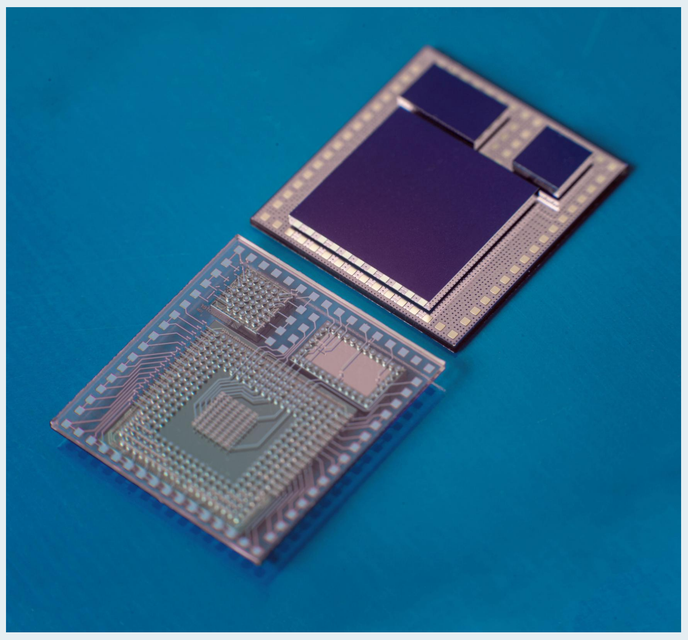

Wafer Level and LTCC Packaging of RF and optical MEMS

TGV wafers are expected to fulfil several requirements of VIS-NIR region optical MEMS device packaging: mechanical protection of fragile MEMS structures, transparency in operational wavelengths and material compatibility to device wafers. Additionally, fabrication platform is relatively mature and modular, thus enabling the integration of TGV-structures to various device platforms. The feasibility of technology and cross-institute piloting collaboration will be demonstrated by capping MEMS-FPI –devices.

LTCC Packaging of RF devices

The objective of the task is to develop and demonstrate novel panel-level capping of RF components utilizing low-temperature co-fired ceramic (LTCC) modules. LTCC technology enables efficient hermetic packaging and integration of active and passive RF devices housed in the LTCC modules. Technology is typically employed in medical applications, automotive industry, space, and communications.

Joint Technology Development

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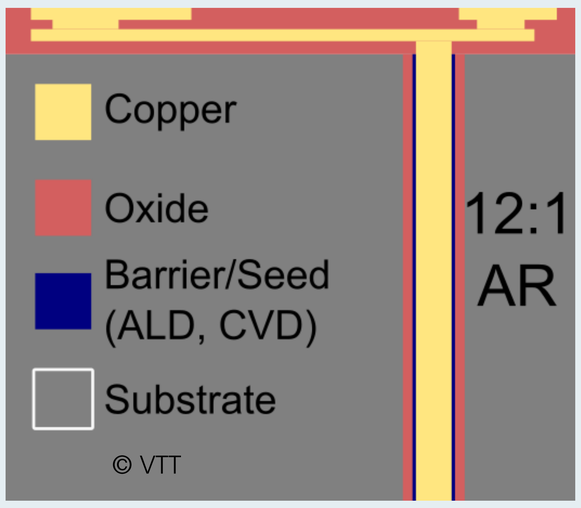
Schematics of Cu TSV with thin barrier and seed layer in used in TSV for the enhanced electrodeposition of copper into the via



Additional information

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