Coordinated by

Fraunhofer

Implemented by

Forschungsfabrik Mikroelektronik Deutschland

Joint Technology Development by INL and Fraunhofer IZM

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Collaborative activities between INL and Fraunhofer IZM are focused on devices exploring 2D Materials.

In particular, the current efforts are to develop and implement a fabrication strategy for 3D heterogeneous integration of CMOS electronics with graphene FET biosensors and with a microfluidic chip. The complete system should consist of:

- A chiplet containing an array of microfabricated graphene field-effect transistors, chemically functionalized to detect particular analytes of interest in real samples
- The samples containing the analytes of interest flow to the graphene sensors using a dedicated microfluidics system, mounted on top of the sensors' chiplet
- The sensors are interrogated using a dedicated CMOS chiplet, heterogeneously integrated below the sensors' chiplet

Detailed schematic of the process flow for the fully integrated 2D Material devices

The figure below shows the process flow devised for the integrated devices.

Detailed process flow to integrate EG-gFETs (INL) with CMOS chiplets (INL and XFAB), and a microfluidics chip (Fraunhofer IZM)
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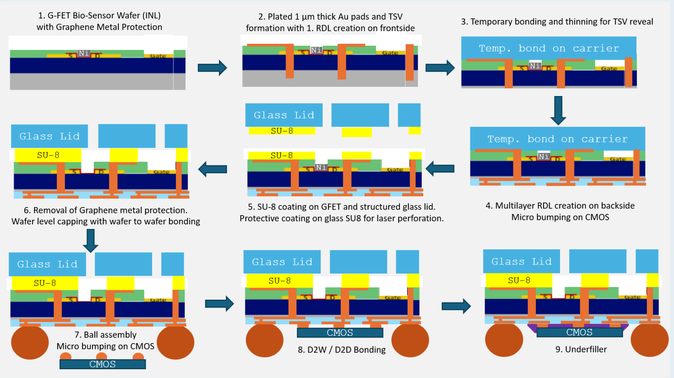

Process flow main steps:

1. INL fabricates the chiplet with the EG-gFETs sensors functionalized to the desired target.
2. INL designs the CMOS chip and fabricates it through XFAB.
3. Both chiplets are sent to Fraunhofer IZM.
4. Fraunhofer IZM integrates both chiplets (sensors and CMOS) using Through-Silicon Vias (TSVs) and Redistribution Layers (RDLs).
5. Fraunhofer IZM fabricates the microfluidics system on top of the EG-gFETs chiplet.
6. The complete system is sent back to INL for testing and biosensing analysis.

Detailed schematic of the EG-gFETs chiplet developed at INL

The figure below shows the detailed schematic of the gFETs developed at INL. It consists of:

1. Hundreds of 5 x 5 mm chips are fabricated on a 200 mm silicon wafer.
2. Each chip contains 256 EG-gFETS disposed in a meander pattern.
3. Individual EG-gFETs with a channel size of 75 x 25 µm .
4. The EG-gFET chiplet contains opening pads for contacting the CMOS chiplet through TSVs.
5. Inlet/Outlet openings with diameter of 500 µm for connection with the microfluidics chiplet mounted on top.
6. Microfluidic channel with a width of 600 µm.

Complete schematics of the EG-gFET sensors' chiplet, developed and microfabricated at INL
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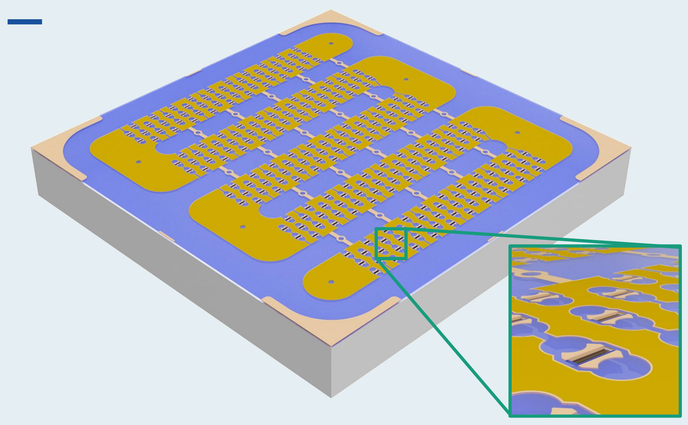


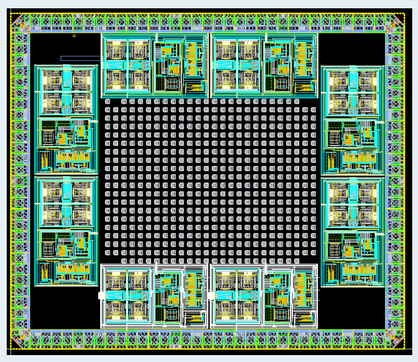
Detailed schematics of the CMOS chiplet, for heterogeneous integration with the EG-gFET chiplet

A CMOS front-end featuring time-multiplexing of 256 devices at a sampling rate of 16 kS/s per sensor, designed at INL, is fabricated in commercial 180 nm CMOS technology at XFAB

The figure below shows a detailed scheme of the CMOS:

1. 120 IO PADs, with passivation openings of 66 µm x 53 µm (standard) and pitch of 98 µm.
2. 513 top contact array in area of 1.92 mm x 1.47 mm (256*(1D+1S)+1G = 513 contacts).
3. Opening of 36 µm x 36 µm, and a pitch of 75 µm.
4. Back area of the contact array reserved for routing and simple digital circuitry.
5. Front-end circuitry and capacitive circuits placed around the contact array.

Top view of the CMOS chip, to be integrated with the sensors' chiplet
© Designed and developed at INL, fabricated at XFAB

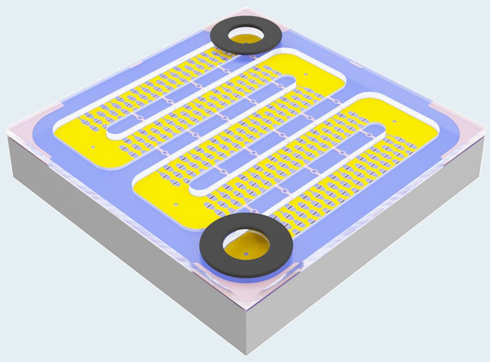


Detailed schematic of the microfluidics to be mounted on top of the sensors' chiplet

The figure below presents the proposed design for the microfluidics chip to be mounted on top of the sensors. It contains:

1. 50 µm high and 600 µm wide meander channel to cover most of the chip.
2. Microfluidic interface/adapter: CapTite Bonded-Port Connector with an Inlet diameter of 1 mm and outer diameter of 2.8 mm.

Complete schematics of the EG-gFET sensors' chiplet, with the microfluidic interface developed at Fraunhofer
© INL

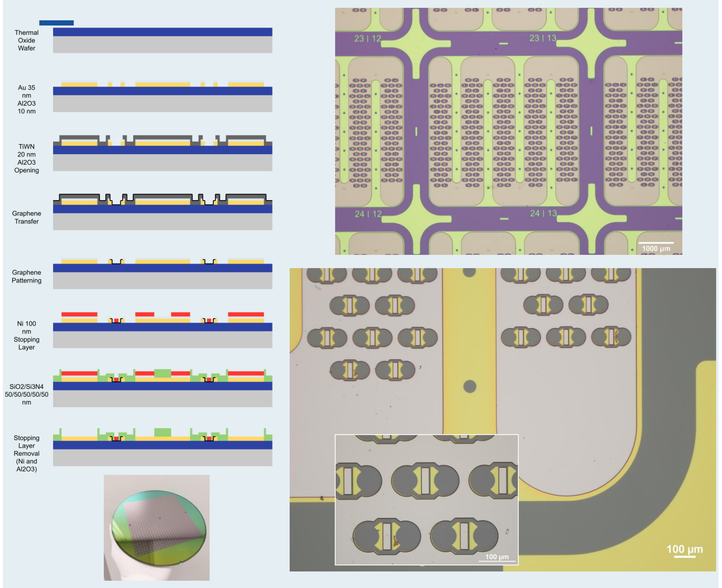


Fabrication of EG-gFET chiplets for initial integration tests with CMOS dummy wafers

A first dummy EG-gFET wafer run was initiated at INL. These wafers will be sent to IZM for initial tests of opening vias through silicon to contact the EG-gFET and CMOS chiplets. The initial designs contain:

1. Patterned gold electrodes.
2. Transferred and patterned graphene channels.
3. Nickel layer to protect the graphene channels during subsequent processes.
4. Silicon nitride passivation layer to protect gold contacts.

EG-gFETs initial dummy wafers to start the testing of heterogeneous integration with CMOS chips
© Design and fabrication at INL, to be sent to Fraunhofer IZM



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Additional information

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