APECS

Coordinated by Fraunhofer

Implemented by Forschungsfabrik Mikroelektronik Deutschland

Joint Technology Development by FORTH and Fraunhofer IZM

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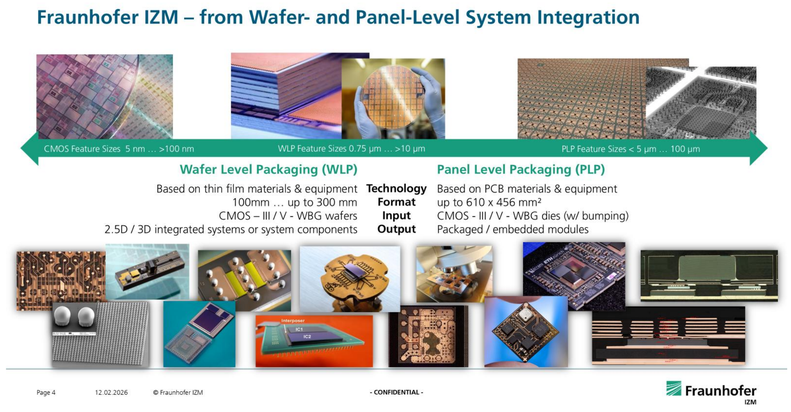
Fraunhofer IZM collaborates with the **SMARTEC pilot line of the Foundation for Research and Technology (FORTH**) to develop, for the first time, 3D sequential integration for analog RF circuits and eventually offer this technology to the APECS pilot line ecosystem & beyond.

SMARTEC pilot line @ FORTH

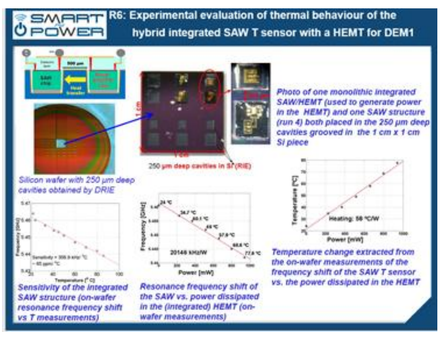
The SMARTEC pilot line is the result of a FTI EU project and focuses on III-V MMICs, RF MEMS and their (monolithic) integration

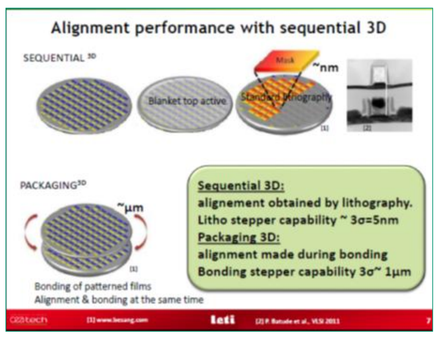
Wafer Level System Integration @ Fraunhofer IZM

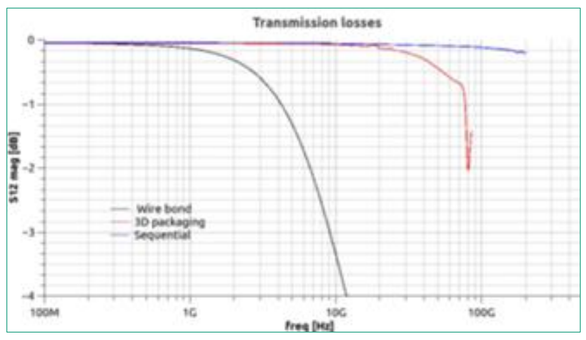


The department Wafer Level System Integration (WLSI) develops advanced packaging and system integration technologies and offers customer-specific solutions for microelectronic products in the overall scope of smart system integration.

Rationale for Task 5.7







Proven past successful collaboration (FORTH & WLSI)

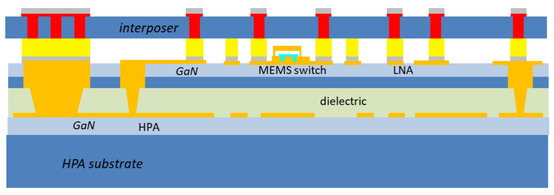
3DSI in analogue RF systems promises to dramatically reduce losses due to much shorter interconnects (ADS) & improve RF performance especially above 30GHz

Main application: SiP RF front ends for radars and communications

3D Sequential Integration (3D SI) of GaN & RF MEMS based RF front end (RFFE) chips

3DSI concept & **Main challenges:**

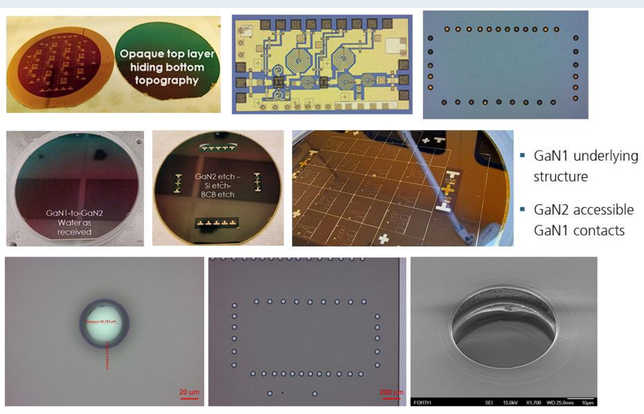
- Wafer-to-wafer stacking of GaN wafers **(voids, thermomechanical)**
- Si, SiC and SI GaN substrates **(HPA functionality & reliability)**
- Sequential processing of GaN wafers **(LNA ohmic contact/laser annealing)**
- TSV formation & filling **(voidfree TSV filling, low RF losses)**
- Hermetical Sealing of MEMS with silicon interposer **(device reliability)**



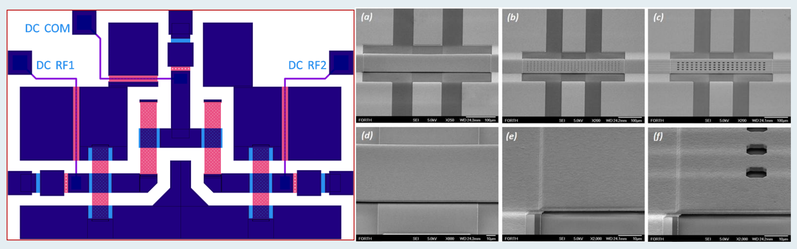
Main Results

GaN1-to-GaN2 via technology

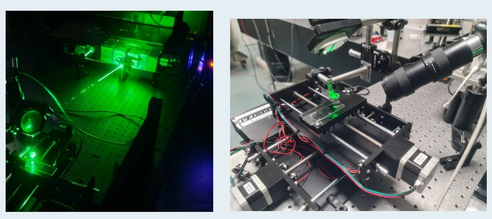
- Etch GaN2, Thin Si on GaN2 substrate and BCB between GaN1 and GaN2
- Multi gas chemistry ICP etching (BCl3/Cl2 for GaN2, SF6/Ar for Si & O2/SF6 for BCB

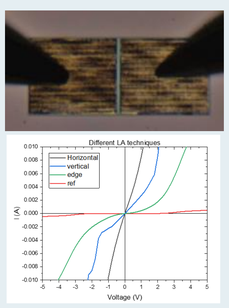


RF-MEMS based SPDT



LA ohmic contacts





Potential Impact

TELECOM

- Higher data rates
- Higher capacity
- Smaller antennas

RADAR

- SWaP & Multifunction systems
- Increase range & resolution
- Faster switching

Alignment with APECS main objectives

- ✓ Next generation technologies for advanced packaging and heterogeneous integrated systems
- ✓ Advanced packaging concepts for communication in small form factors
- ✓ New process modules, to ensure quality, reliability and security of heterogeneously integrated chips and systems
- ✓ New design methodologies for heterogenous integrated systems in a single package with improved performances (power, higher frequency, less energy consumption)
- ✓ A sustainable pilot line, open to European stakeholders (especially for SMEs and start ups) from the entire value chain
- ✓ Skills development

Next Steps (Q3 & Q4 2026)

1. LA ohmic contact further optimisation
2. Finalize GaN1-to-GaN2 stack process with existing design
3. Test functionality

Joint Technology Development

FORTH Fraunhofer IZM

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Additional information

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