APECS

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Implemented by Forschungsfabrik Mikroelektronik Deutschland

Demonstrator 4: Radio Frequency Integration (RF)

Integration of III-V semiconductor components for radar and mobile communication applications

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Four Sub-Demonstrators for one Mission

In the field of complex, highly integrated RF systems, four technology sub-demonstrators will be implemented to demonstrate the performance and innovative potential of various combinations of semiconductor and heterogeneous integration technologies. The addressed applications range from next-generation mobile communications and wireless links to advanced radar systems. Particular emphasis is placed on the practical validation of the design enablement developed within APECS (including PDKs, ADKs, and design tools), as well as on the experimental verification of the capabilities developed, including testing.

1. InP-on-BiCMOS TRX: 6G D-Band Transceiver

The D-band (110…170 GHz) offers large absolute bandwidth for wireless communications as needed, e.g., for high-data rate point-to-point links in the backhaul network of 5G and 6G base stations. Hetero-integration of bipolar InP chiplets with BiCMOS boosts D-band output power and efficiency, thus extending range and energy efficiency. PA and switch are realized as chiplets in InP-HBT technology, the other subcircuits of the TRX in SiGe-BiCMOS. The approach provides seamless integration of the two technologies with broadband interconnects using microbumps. It allows for array scalability. The sub-demonstrator will present a four-channel solution.

InP chiplet mounted on SiGe BiCMOS wafer
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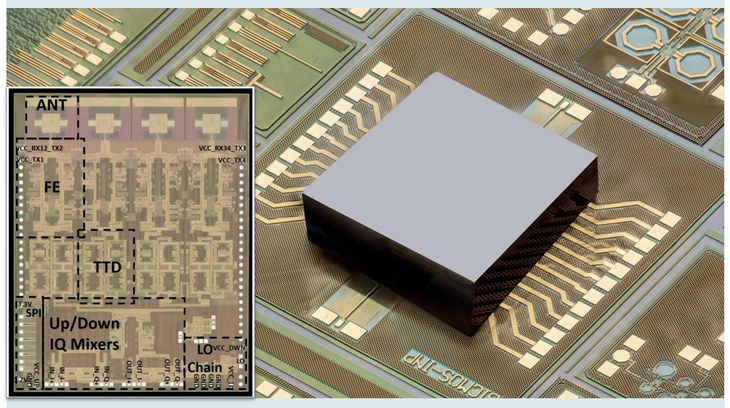

2. Sub-THz BiCMOS-mHEMT Transceiver on Interposer

The sub-demonstrator #2 targets heterointegration-based sub-THz chiplets and interposer technologies for high-resolution sensing. The sub-demonstrator aims to realize a high resolution FMCW radar front-end operating at 256 GHz by combining a SiGe BiCMOS transceiver chiplet based on a flip-chip assembly with copper pillars/Al-Al bonding together with InGaAs mHEMT LNA/MPA chiplets using indium micro-bumps (for flip-chip assembly as well) on a common interposer. A central goal is the use of fused silica and silicon interposers to demonstrate a scalable, low-loss, compact and modular platform for sub-THz systems-on-interposer.

Indium Microbumps and Thru-Substrate-Vias on Fused Silica
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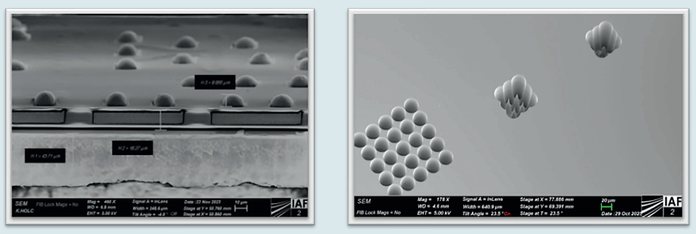
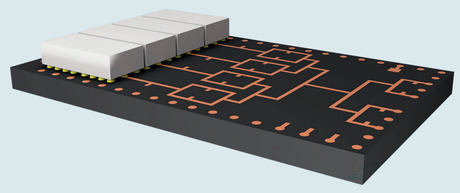
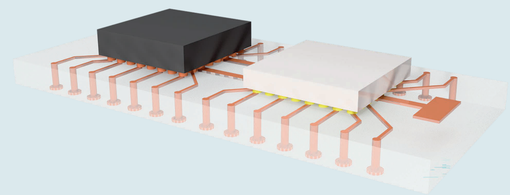


Overview of the four Demonstrators for Radio Frequency

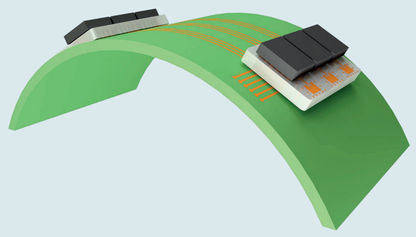
#1: InP-on-BiCMOS transceiver (TRX)



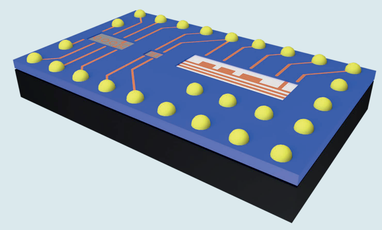
#2: Sub-THz BiCMOS-mHEMT Transceiver[RM19.1] on Interposer



#3: D-Band Multi-Module-Radar on Flex Interposer



#4: D-band communication module

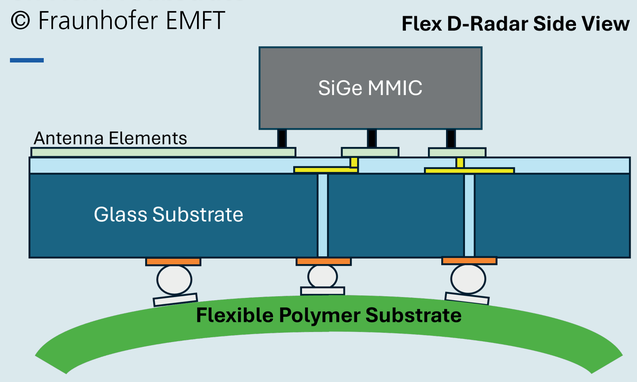


3. Flex D-Band Radar

Compared to Sub-demonstrators #1 and #2, the Flex D-Band Radar aims to showcase the pilot line's capabilities in integrating a multi-module radar system onto bendable and/or non-planar surfaces. The concept is based on a heterogeneously integrated D-band radar transceiver mounted on an RF-glass interposer using flip-chip technology. In addition, broadband TX and RX antennas will be implemented on the RF-glass interposer and connected to the radar chiplet via low-loss interconnects.

This approach offers significant advantages over on-chip antennas, including higher efficiency and wider bandwidth. These radar modules—each consisting of a D-band frontend and an RF-glass interposer with an antenna array—will be integrated multiple times onto a flexible polymer interposer. The resulting innovation is a multi-module radar system that is well suited for integration into or onto bendable and/or non-planar surfaces, such as the wings of wind turbines or drones to give just a few examples.

RF Radar Module (Radar Frontend on RF-Glass) on Flex PI substrate
© Fraunhofer EMFT



4. D-Band Communication Module

In alignment with sub-demonstrator #3 above, sub-demonstrator #4 is also guided by the goal to show the integration of multiple chiplets. Here, a fan-out wafer level packaging (FOWLP) approach will be presented. FOWLP is well suited for RF and mmWave application due to shortest interconnects and feasibility of passive components and structure integration. The package will co-integrate two technologies: gallium nitride (GaN) and advanced FDSOI CMOS. Also cooling structures are integrated to ensure long-term stability of the integrated chiplets.

GaN Power Amplifier (PA)
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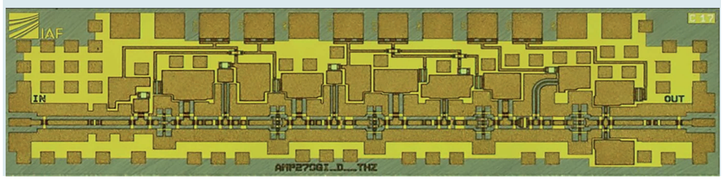

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Additional information

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