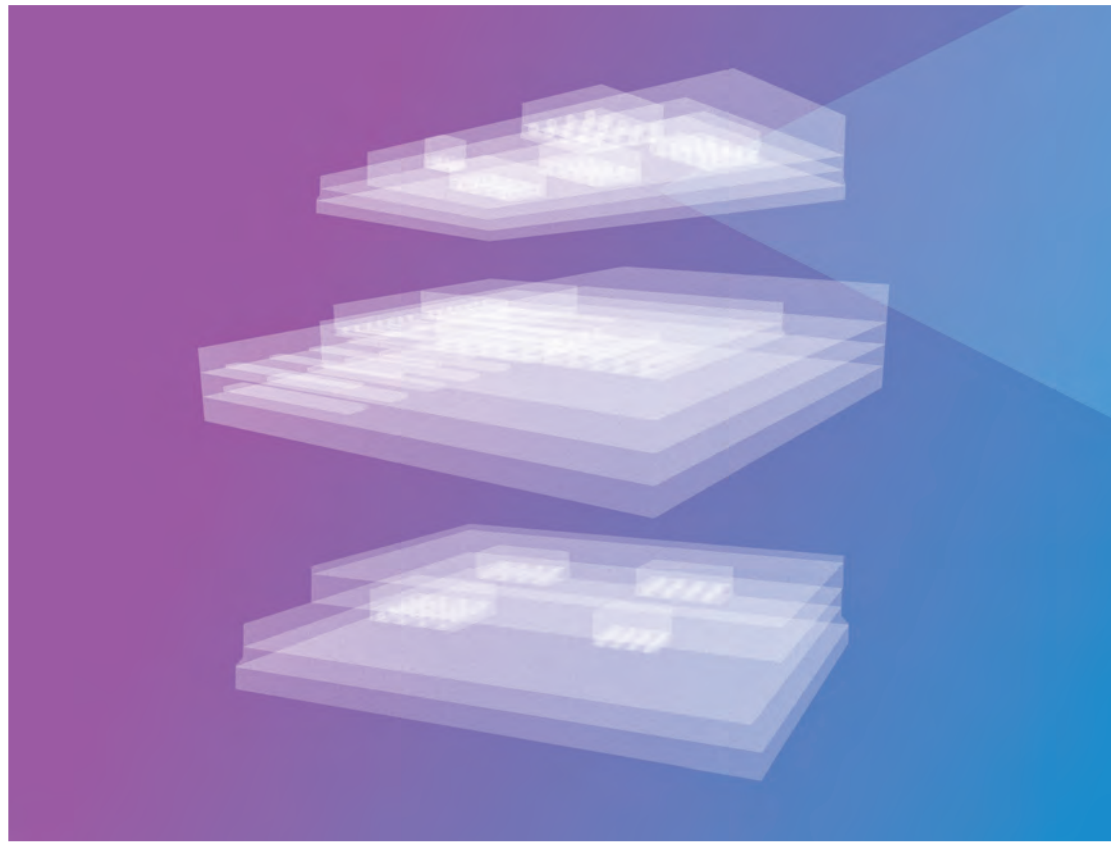


HPC Computing Module



Areas of Application



Industry & Automation



Medical Technologies



Data Centers / HPC



Security

High Performance Computing

Multi-Material Sensor

Photonic Integration

Radio Frequency Solutions

coordinated by

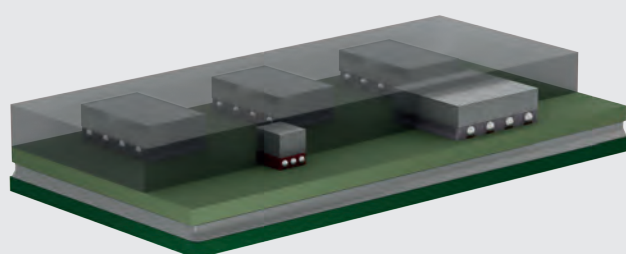


implemented by

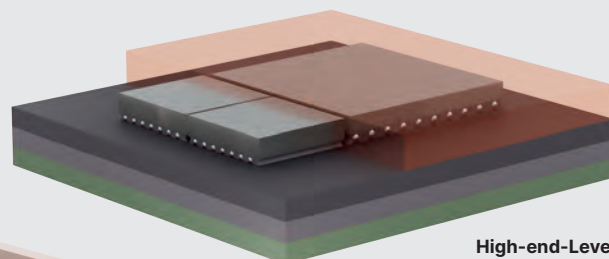


**Co-funded by
the European Union**

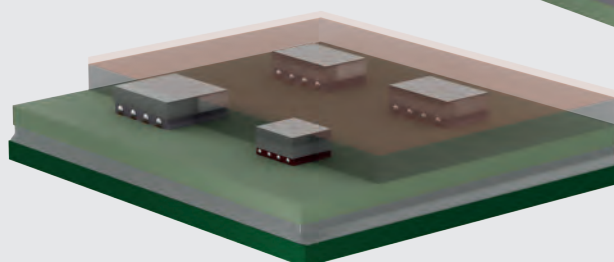
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Entry-Level



High-end-Level



Midrange-Level

The **High-Performance Computing (HPC)** demonstrator focuses on components for high-performance computing system modules, aiming at high integration density and high data transmission rate within the modules. State-of-the-art technologies are applied within the workflow and designs of the individual components. Furthermore, customer requirements such as cost, size, and energy consumption are incorporated directly into chiplet and chip design, using System-Technology Co-Optimization (STCO) systematics. Therewith, scalable production and reliable performance at short development time are achieved.

Within the HPC demonstrator, different levels of performance are addressed:

HPC computing modules built on silicon chiplets on an Entry-Level HDI-PCB organic Substrate as Interposer

AI flip chip package assembly, combining a RF chiplet and 3 neural processing unit chiplets.

HPC computing modules built on silicon chiplets on a Midrange-Level HD organic Substrate as Interposer

Data center flip chip package assembly with thermal management, combining a periphery chiplet, security chiplet, and 3 RISC-V multicore chiplet.

For both, organic package substrates are applied as interposers. This enables bandwidth densities around 100 GB/s/mm² according to the UCle-S standard.

High-end-Level Silicon Interposer demonstrated in an assembly with dummy chiplets

Addressing the future needs for significantly greater bandwidths, the STCO flow for ultra-high density (UHD) heterogeneous integration is transferred on 300 mm Si wafer level. Since the interfaces between foundry-manufactured wafers and the integration of respective chiplets into next gen HPC systems lack the required rigorous definitions, the targeted technology demonstrator has no compute function but will implement several leading-edge advanced packaging technologies, such as ultra-high density redistribution layers with integrated capacitors and resistors to support signal integrity and power supply, as well as high-density mixed-pitch interconnections based on hybrid bonding and microbumps to enable bandwidths above 1 TB/s/mm² according to UCle-A and UCle-3D.

