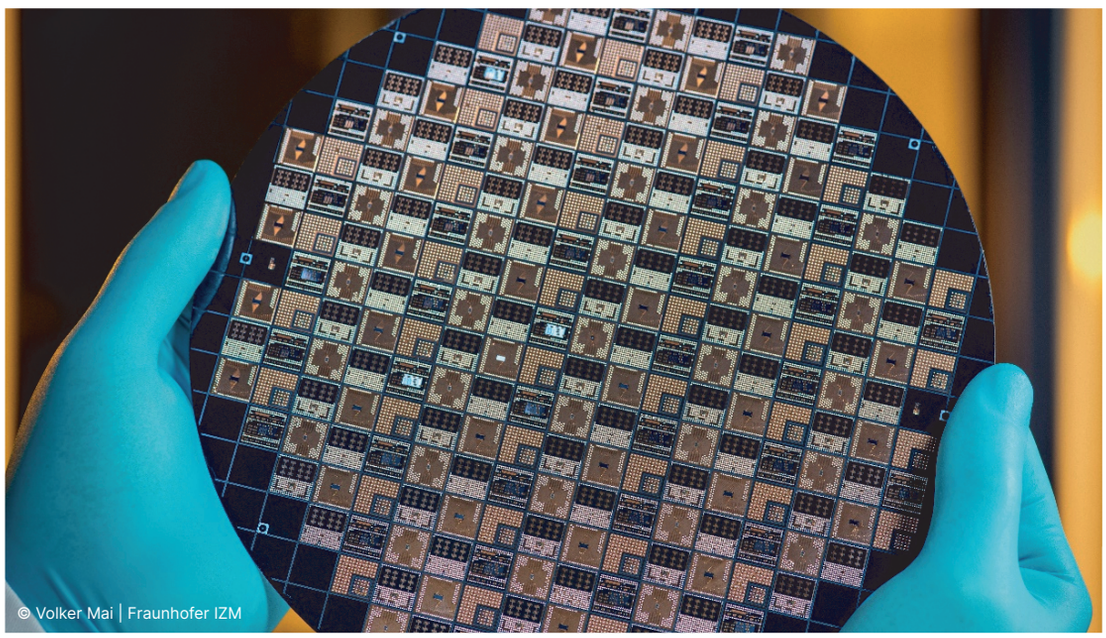
APECS

Multi-Project Wafer Prototyping Chain

From sub-THz silicon-based BiCMOS dies to RF-optimized System-in-Package



High-speed SiGe:C BiCMOS dies (SG13G3Cu) ready to be carried to the board by Fan-Out Wafer Level Packaging (FOWLP)

The European Pilot Line for Advanced Packaging and Heterogeneous Integration of Electronic Components and Systems (**APECS**) offers edge SG13G3Cu SiGe:C BiCMOS ICs as high-quality and cost-effective system-in-package prototypes for radar, communications and sensor systems operating at D-Band and beyond. Two Multi-Project Wafer Runs at IHP and Fraunhofer IZM are synchronized to manufacture optimised RF-system-in-package solutions in small volumes.

Unique Selling Point

- Service combination from two Multi-Project Wafer Runs at IHP and Fraunhofer IZM to manufacture RF-system-in-package solutions in small volumes, enabling research institutes, universities, SMEs and start-ups to obtain a complete packaged prototype at a fraction of the cost of a dedicated run.
- The timeline of the Multi-Project Wafer Runs is optimally synchronized and coordinated with one customer interface as part of the APECS Pilot Line.

more information

Benefits

- **SiGe-BiCMOS performance**: RDL-last and microvias replace long bond wires and provide the shortest interconnect path, resulting in ultra-low parasitic values that maximize signal integrity and high-frequency transistor performance across fan-out variants.
- **More I/Os without a larger die**: Fan-out routing extends beyond the chip footprint, adding RF, DC and digital connections without needing to enlarge the die solely for pads.
- **Compact and thin**: thin package, no laminate substrate – ideal for advanced packaging for 5G / 6G.
- **Standard PCB assembly**: BGA mounting using conventional reflow soldering simplifies PCB assembly and reduce costs compared with bare-die mounting and RF wire bonding.

Applications

- **Wireless communications**: RF frontends for 5G infrastructure, terminals and emerging 6G systems.
- **Optical communications**: High-speed transceiver electronics.
- **Advanced sensing and imaging:** mmWave and sub-THz systems for industrial sensing, security screening and spectroscopy.
- **Test and measurement:** High-frequency instrumentation and measurement systems.
- **Aerospace and defence:** RF communication, radar and sensing frontends.

Our Offer

- Die fabrication on IHP's Multi-Project-Wafer service.
- Package design according to fixed Multi-Project Wafer Level Packaging design rules, including RDL planning for potential passives and antennas.
- Chip-package co-design advice on pad layout, die-to-RDL transition and die thinning.
- Fabrication of the reconfigured 200 mm fan-out wafer, including molding, RDL structuring, under bump metallization, balling and singulation at Fraunhofer IZM.
- 30 packaged chips as engineering samples – early access is standard offer.
- Full cycle-time of 10 months (first run in July 2027)

APECS

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