

# Joint Technology Development by imec and Fraunhofer ENAS, IMWS & IZM

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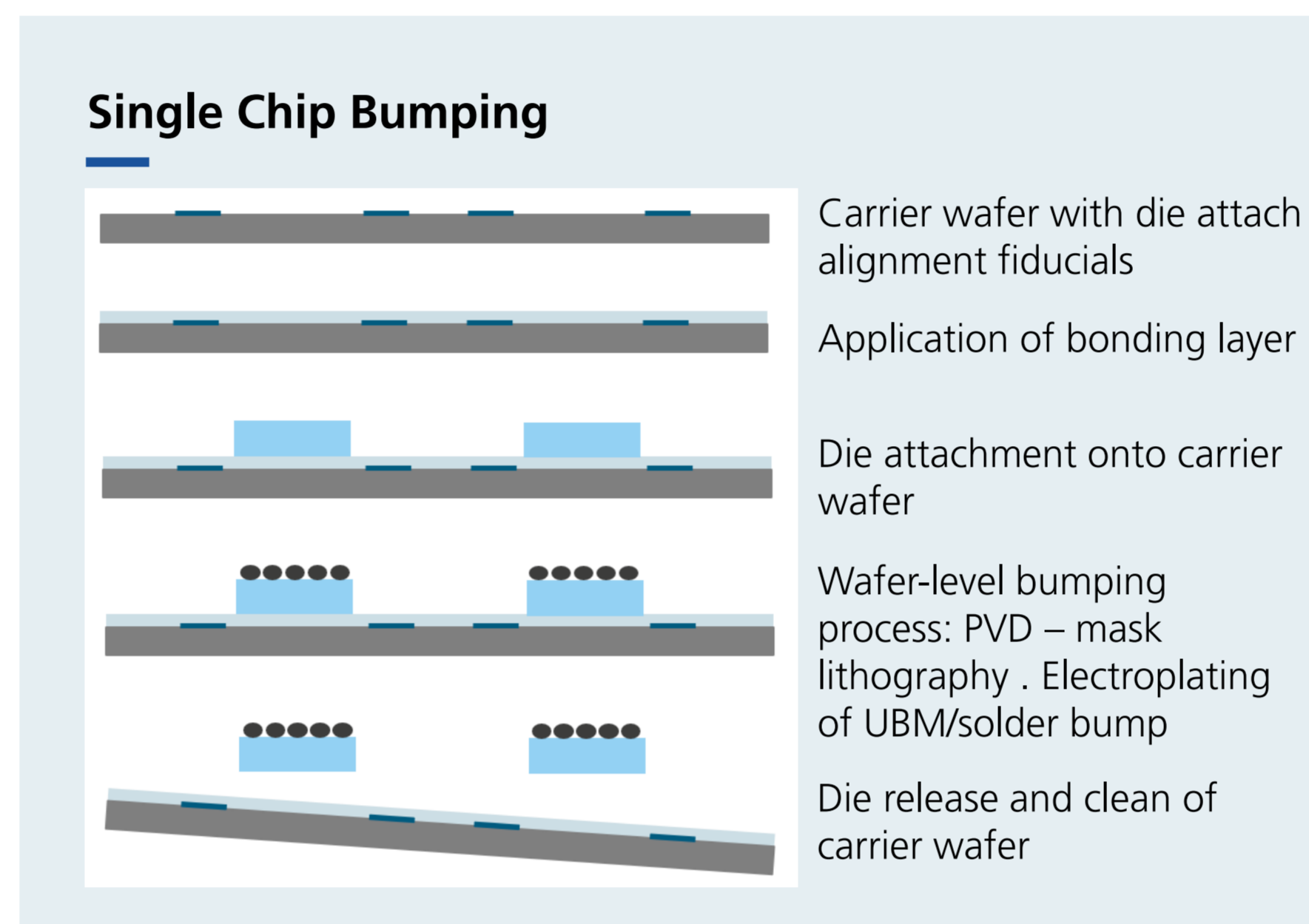
## Work Package Overview

The two institutions involved in this topic, imec and FMD, have the needed infrastructure, employing complementary technology building blocks, i.e. multi-layer RDL, 3D stacking and overmold vs. singulated chiplet  $\mu$ -bumping, 2.5D assembly, molding and packaging. The study will cover a variation of chiplet size and interconnect density. The primary objective is to assess the technological capabilities to be engaged for an EU cooperation pilot line.

The process starts with the RDL 1<sup>st</sup> realization on a carrier wafer, the chiplet assembly is done (featuring a mix of bump pitches of 40 $\mu$ m, 50 $\mu$ m and 100 $\mu$ m) at both RTO sites with different die thicknesses. Molding is carried out afterwards, whereas the mold cap is thinned down until revealing chiplet back sides. After carrier release, balling and board assembly is done. To optimize the performance of the package, test chips are developed (with integrated heater, temperature sensor, stress sensor, humidity sensor), that mimic different heating schemes (heat spots or larger heated areas) and new thermal management concepts will be integrated (SiC as heat spreader, 3D printed fluidic heat dissipation systems).

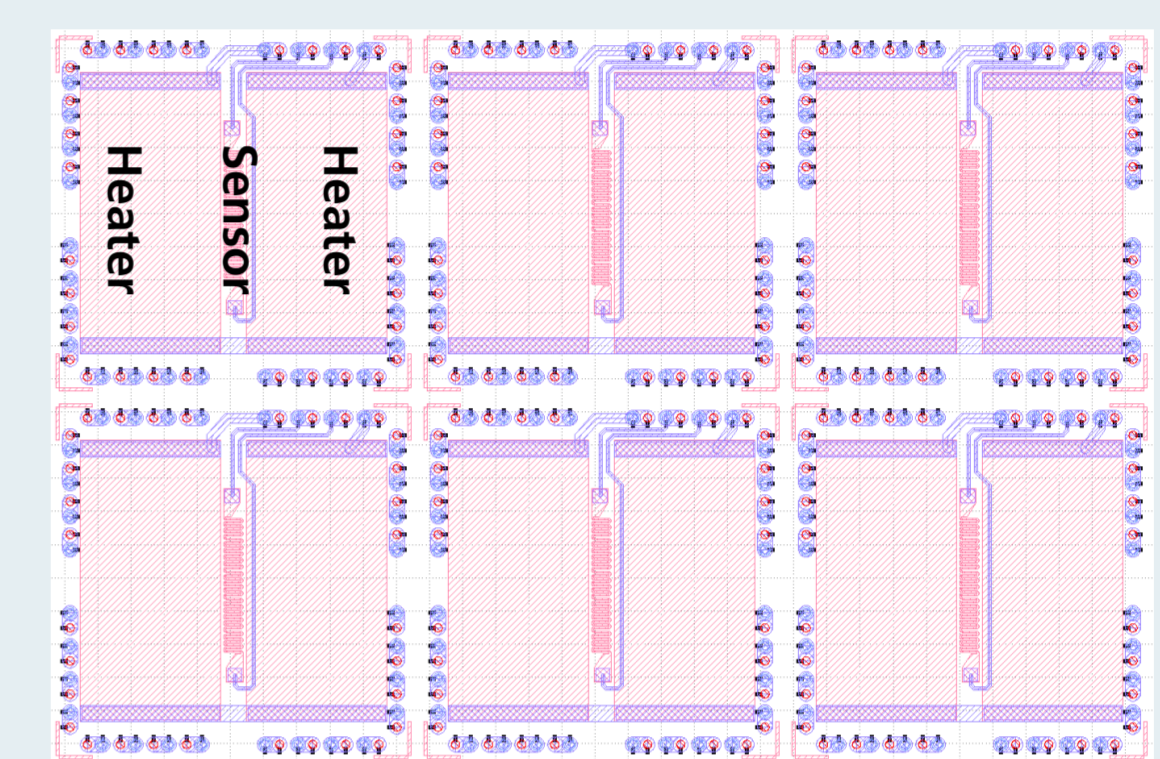
FMD will support the process development by advanced failure analysis to identify process related defects and related failure modes and to adapt innovative defect metrology and analysis methods for novel key technologies like imec's backside power delivery ICs, hybrid bonding, advanced RDL and 3D packaging to support and speed up technology qualification and ramp up. This includes the development of design for failure analysis concepts to enable more efficient and quantified localization of electrical defects within the complex 3D electrical routing of high-performance SiP. The module assembly process flow will be digitized by FMD as a compact digital twin model for virtual process and reliability optimization.

To enable access to the pilot line even with chiplets from multi project wafer runs that have no bumping, Fraunhofer IZM will enhance their single chip bumping capabilities. Concept on FhG side is ready, manufacturing will start beginning of 2026, but the overall process is waiting until end of 2026 for installation of high precision D2W die attach placer (IZM-002.1).



For thermal analysis, test chiplets are being developed to study the behavior of heat spreaders attached to the top side of the package. For this purpose, imec is developing a thermal test die that can be integrated on the RDL interposer, featuring very small heating spots that also serve as a calibration device for the lock-in thermography performed at Fraunhofer IMWS. Based on this starting point, the root causes of failures due to thermal stress are investigated down to the atomic level using high-resolution imaging (HRTEM/STEM) and spectroscopic chemical analysis methods (EELS/ToF-SIMS) at Fraunhofer IMWS. In contrast, Fraunhofer IZM will develop a thermo-/humidity-test chiplet with larger heating areas and higher power output that can be used in a more general fashion (pixelated heating chiplets can be combined into different die sizes) to study heat spreading in FOWLP.

## Thermo-/Humidity-Test Chiplets



## Summary

- RDL 1<sup>st</sup> Packaging Demonstrator process flow is established, starting with several short loop runs between imec and Fraunhofer IZM
- Thermal lock-in thermography is available at Fraunhofer IMWS, stackable thermo-test chips for calibration are in the design flow at imec
- Single chip bumping process concept is ready at Fraunhofer IZM, processing starts in 2026
- Thermo-/Humidity-test chips for package test are designed at Fraunhofer IZM, and first samples are manufactured in 2026
- TEM and ToF-SIMS will be employed to identify the root causes of thermally induced failures at Fraunhofer IMWS
- Digital Twin development is starting at Fraunhofer ENAS in 2026

## Joint Technology Development



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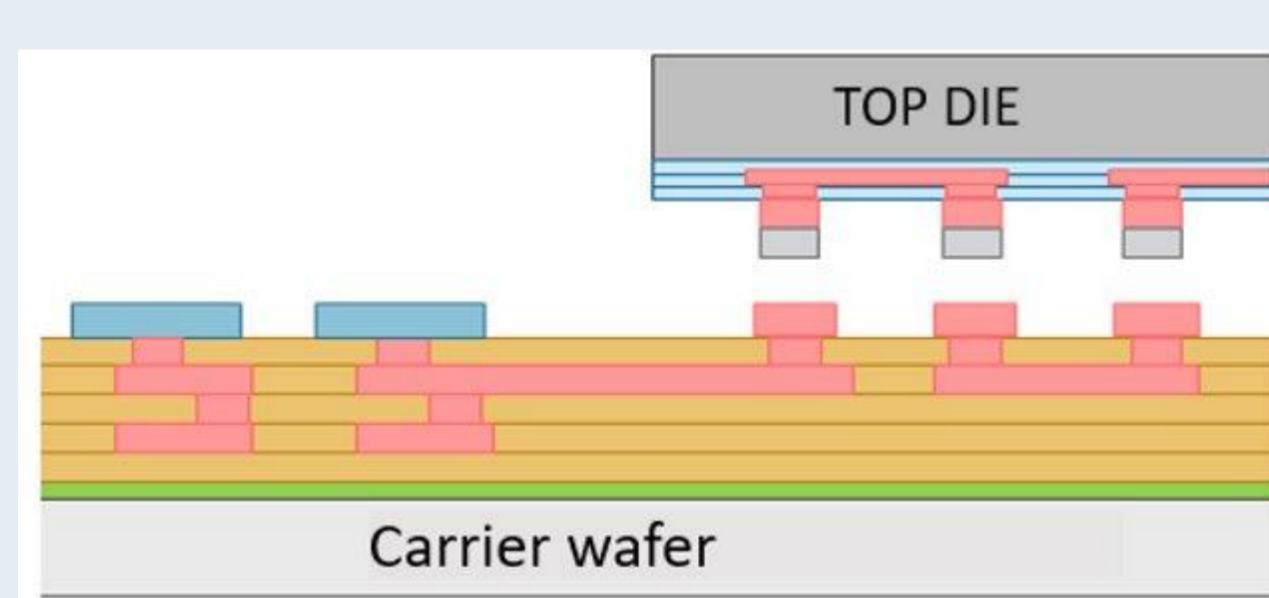
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## Additional information

The work presented was carried out in the framework of the APECS Pilot Line of the Chips Joint Undertaking, funded by Horizon Europe and Digital Europe Programmes and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain.

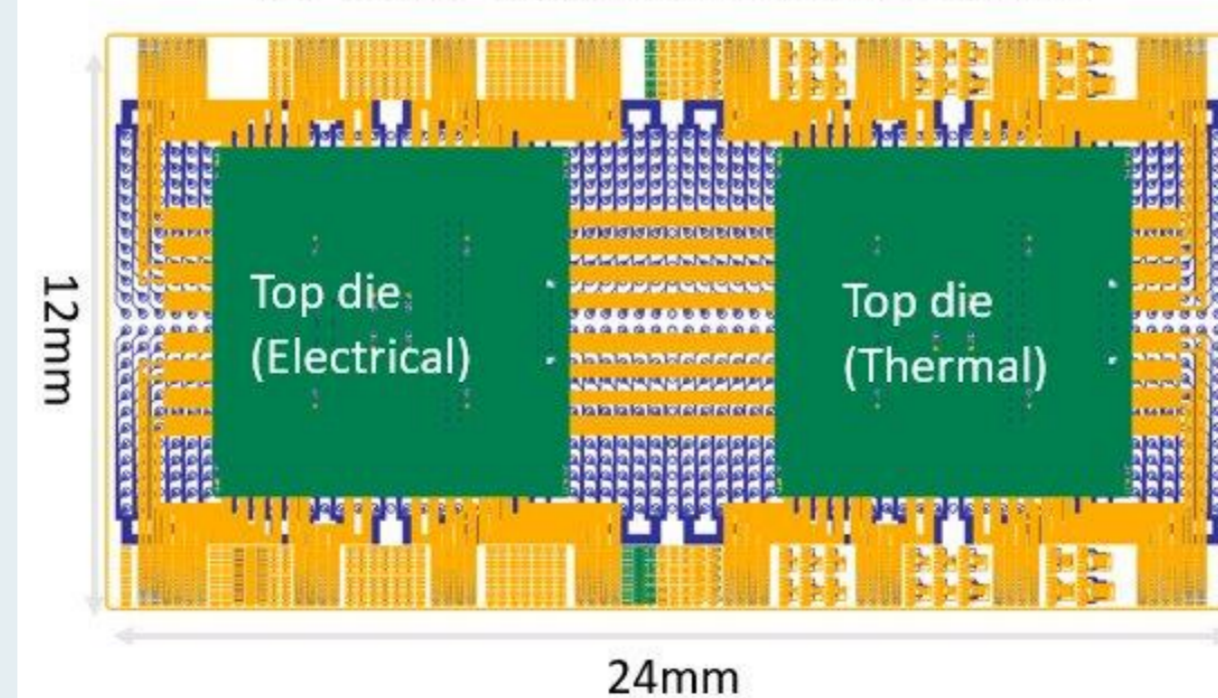
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## Package Design



Cross-Section

## Top view: top die on RDL interposer



Top View

## RDL 1st FOWLP - Process Flow Overview

